GaN power devices: plenty of room at the bottom and the top

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Power semiconductors as pathways to carbon neutrality

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Wide-bandgap semiconductors and power electronics as pathways to carbon neutrality

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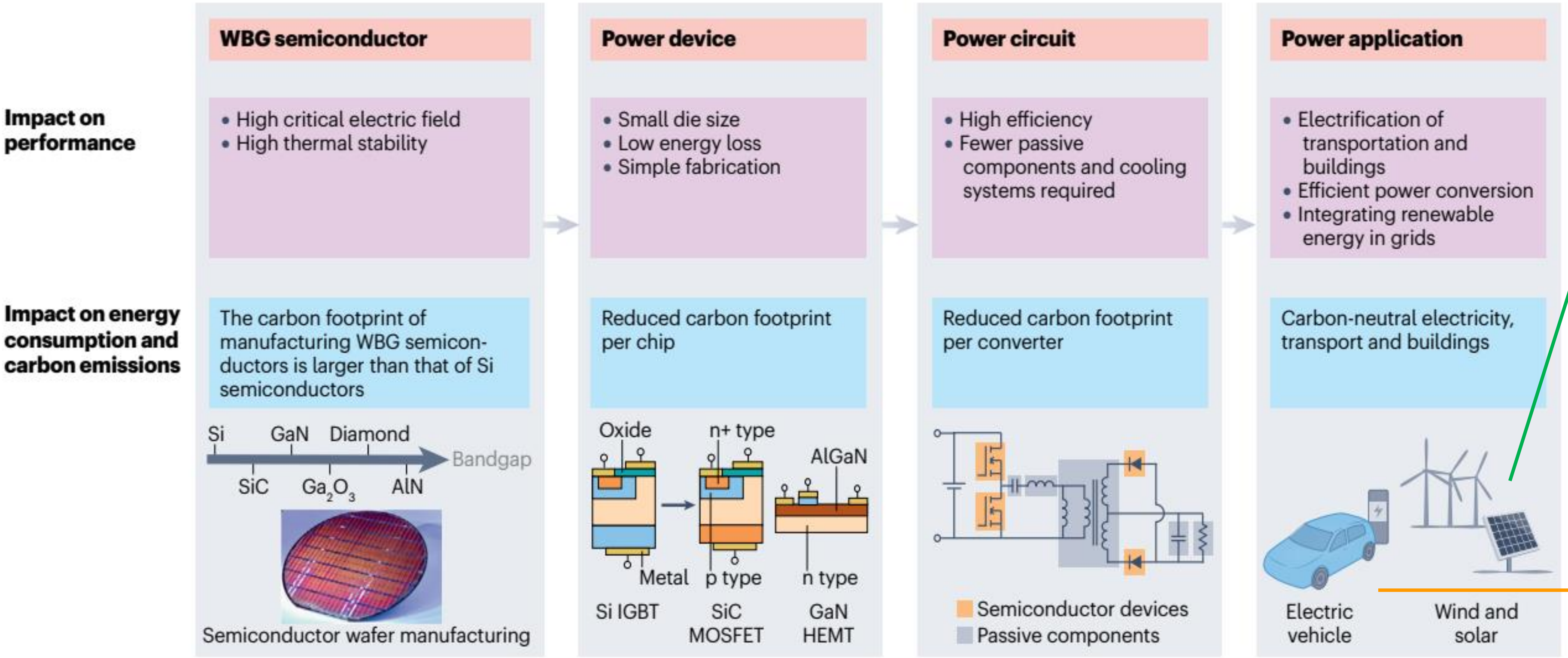
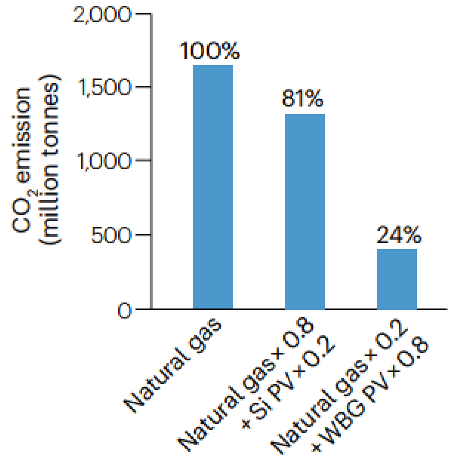
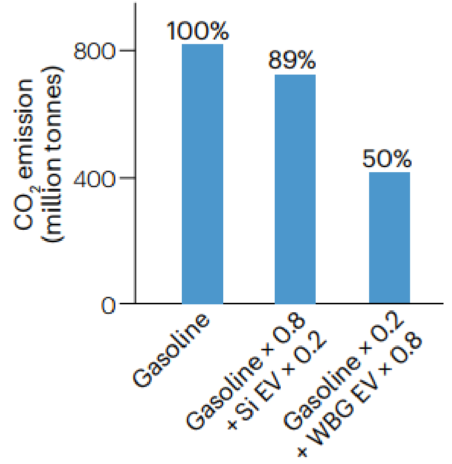
WGB replacing Si can enable an annual carbon saving of at least 20 million tons in the USA – annual emissions of 4 million gasoline passenger vehicles



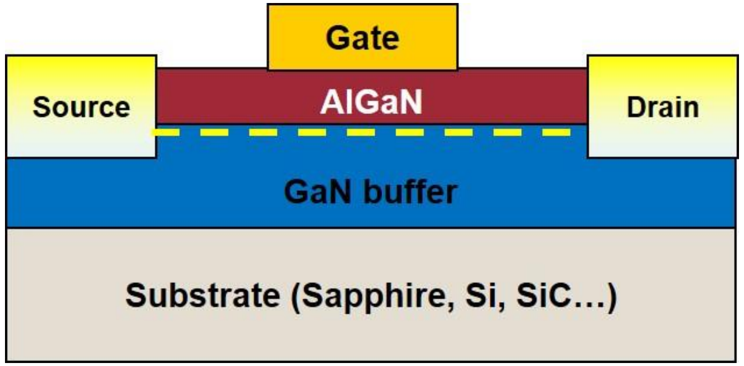
electricity generation



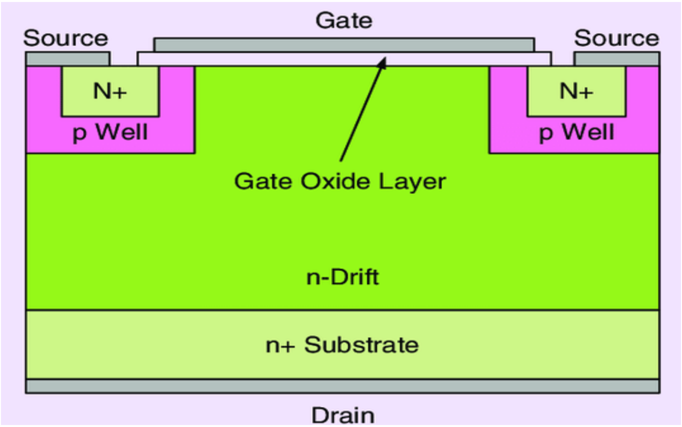
electric vehicles



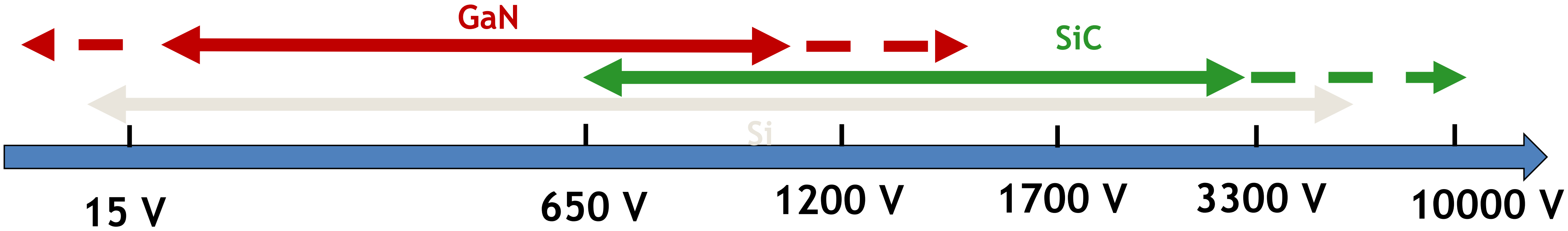
GaN HEMTs and SiC MOSFETs ($10B market by 2027)



- √ 2DEG: mobility >1500 cm^2/Vs
- √ easy for IC integration
- × large chip size for high-voltage
- × thermal and E-field management
- × robustness (avalanche and short-circuit)



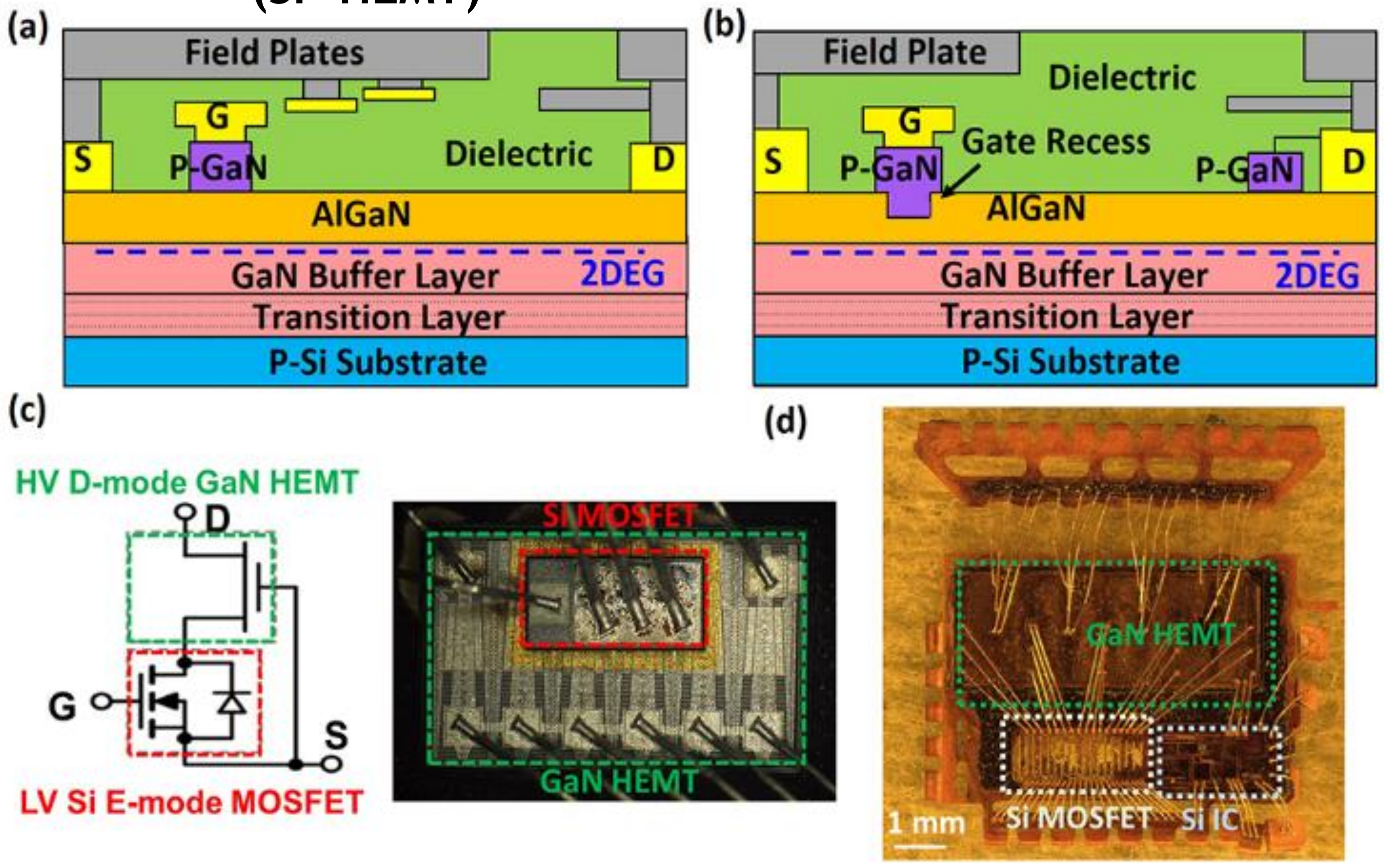
- × MOS: mobility ~100 cm^2/Vs
- × Mostly discrete
- √ high current
- √ small chip size for high-voltage
- √ easier thermal management



Commercial GaN devices

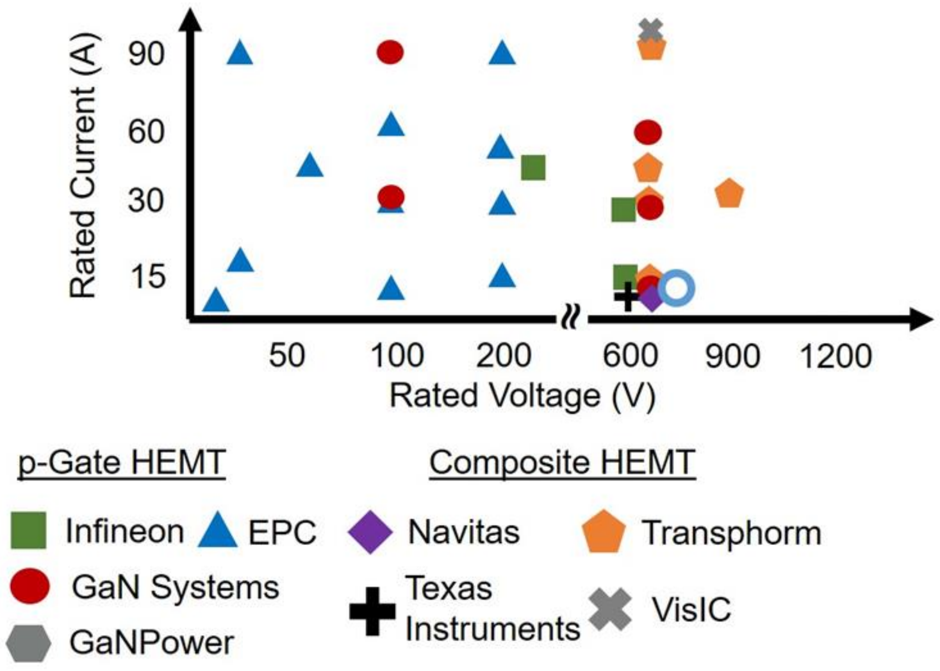
Schottky-type p-gate HEMT (SP-HEMT)

Gate injection transistor (GIT)



Cascode GaN HEMTs

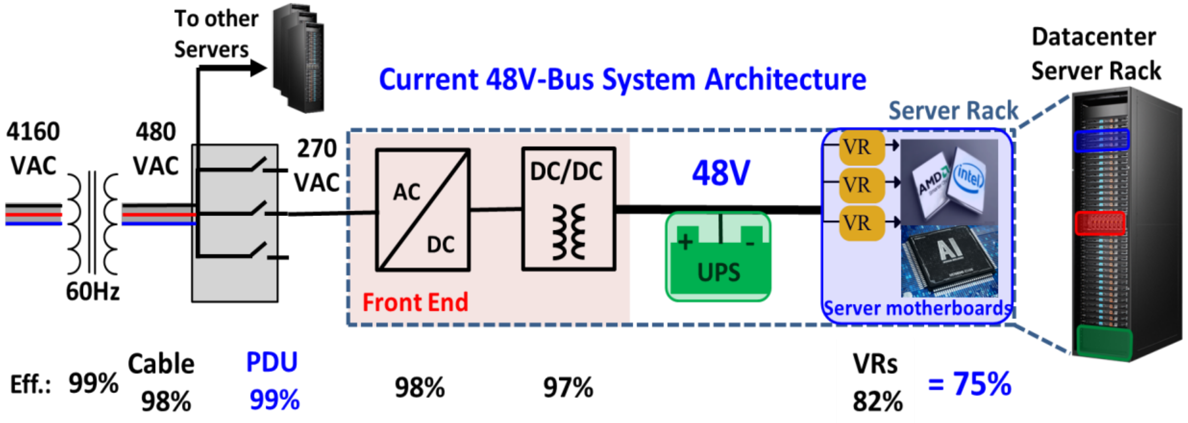
Direct-drive GaN HEMTs

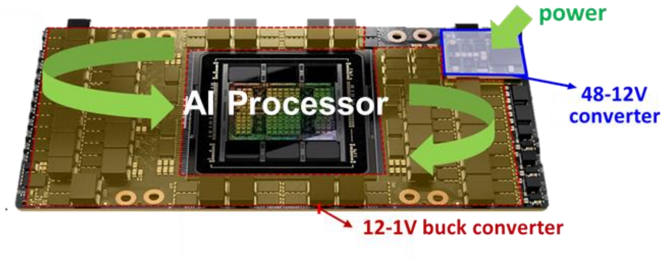


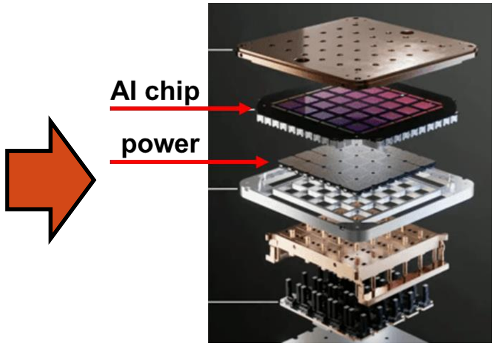
J. Kozak *et al.*, "Stability, reliability, and robustness of GaN power devices: a review," IEEE Trans. Power Electron., 2023

Huge market opportunities at the bottom and the top

LV (<20V) device for AI processor power management

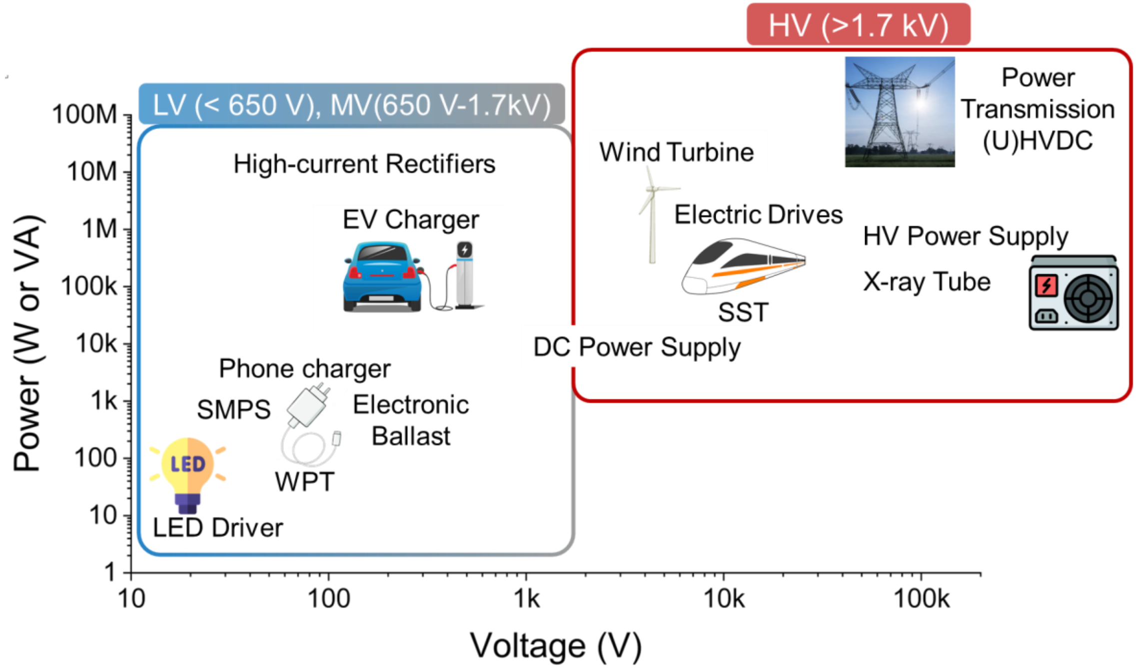






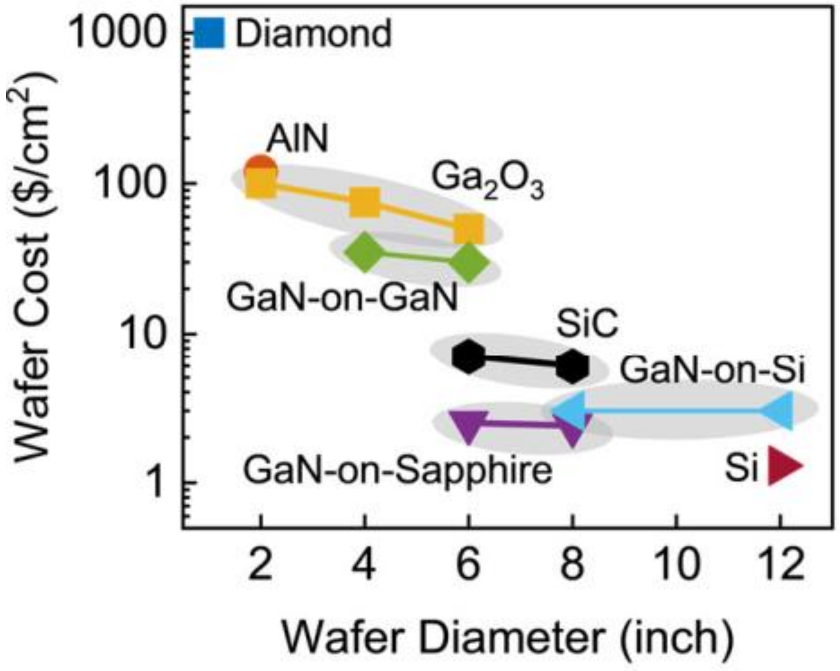
- Lateral -> vertical power delivery
- Requires LV devices and integrated circuits to enable >3~5 MHz system frequency

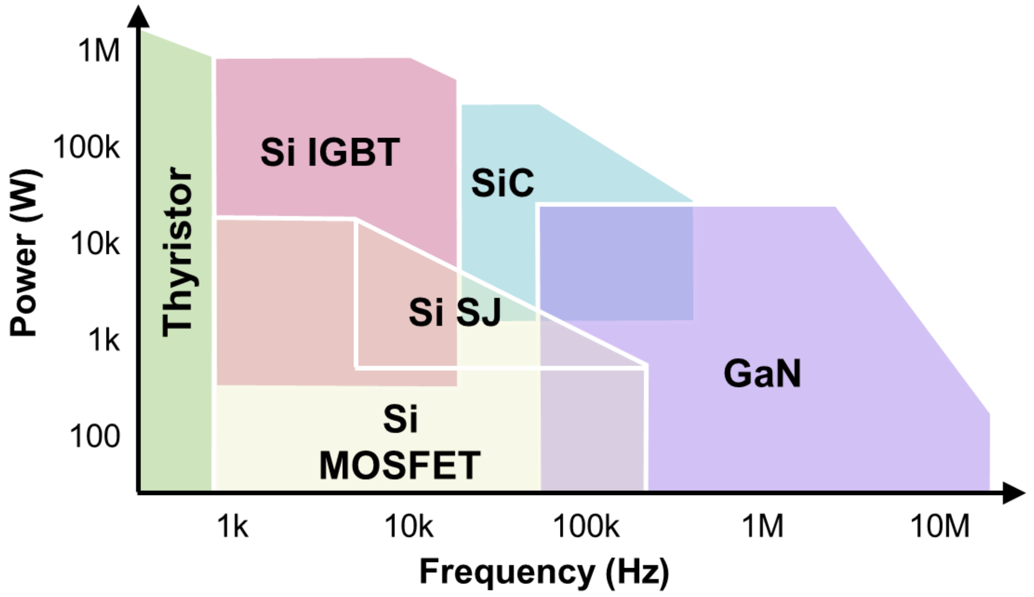
HV (multi-kV) device for industrial applications



- Grid, renewable energy processing, HV power supplies, transportation electrification
- Demand multi-kilovolt devices with current from sub-amp to thousands of amps

Advantages of GaN is largely voltage class agnostic

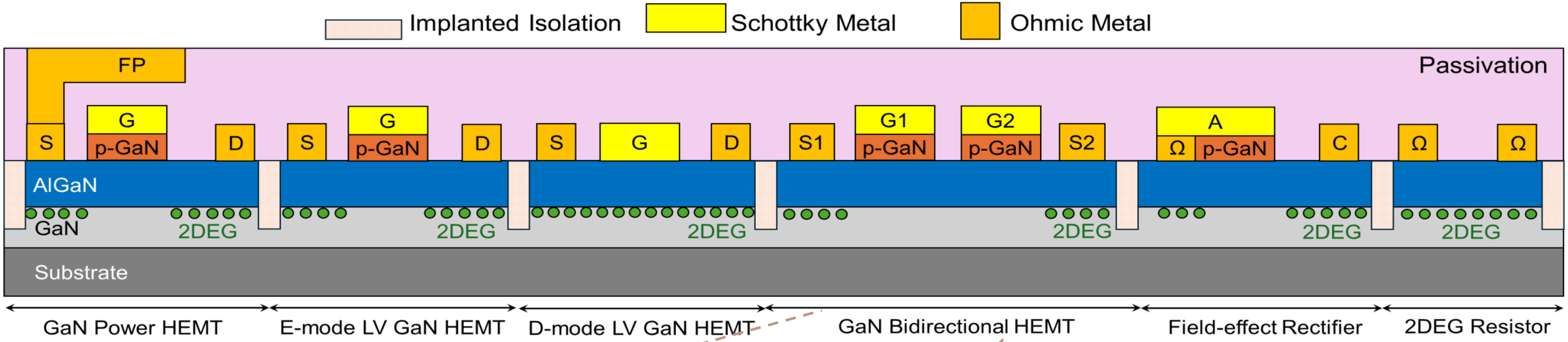


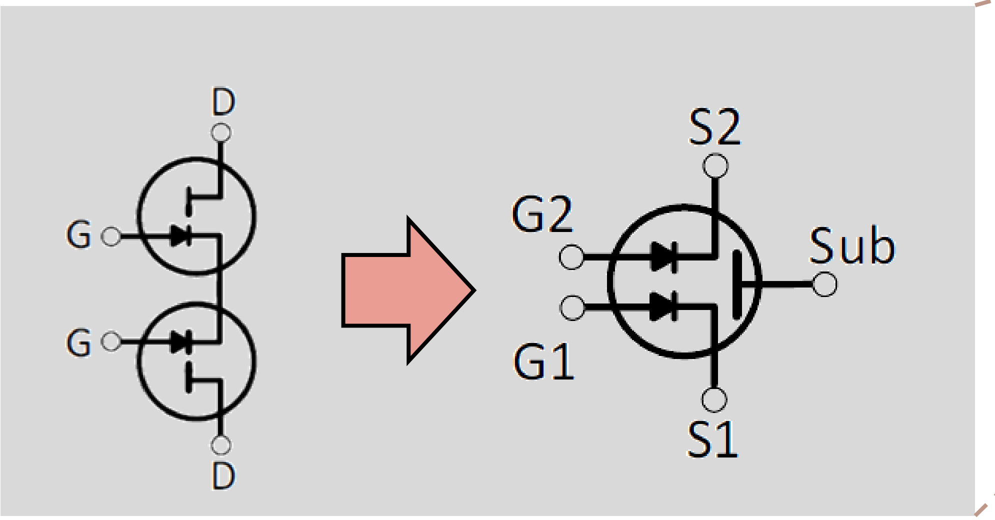


Y. Zhang *et al.*, *Nature Reviews Electrical Engineering*, 2025

- GaN device can be unipolar (fast switching) from 1 V to 10,000 V (in contrast Si only up to 900 V)
- GaN-on-Si/sapphire offers significant cost advantage over SiC
- GaN devices can enable faster switching frequency than Si and SiC
- *How to make GaN power devices suitable for LV and HV applications?*

And… unique capability of GaN (vs. SiC): integration





- GaN enables monolithic integration of power switches with control and driver IC
- **Monolithic bidirectional GaN switch**: a single device replacing two discrete devices, offering at least 4x savings in device area (and cost)

Outline

- *How to make GaN device better for LV and HV?*
  - Multidimensional architecture
  - FinFET, superjunction and multi-channel
  - New theoretical limits and scaling laws
- *What system benefits can new GaN devices enable?*
  - Dynamic R_{ON} free, avalanche and short-circuit robust
  - Kilovolt, megahertz soft switching

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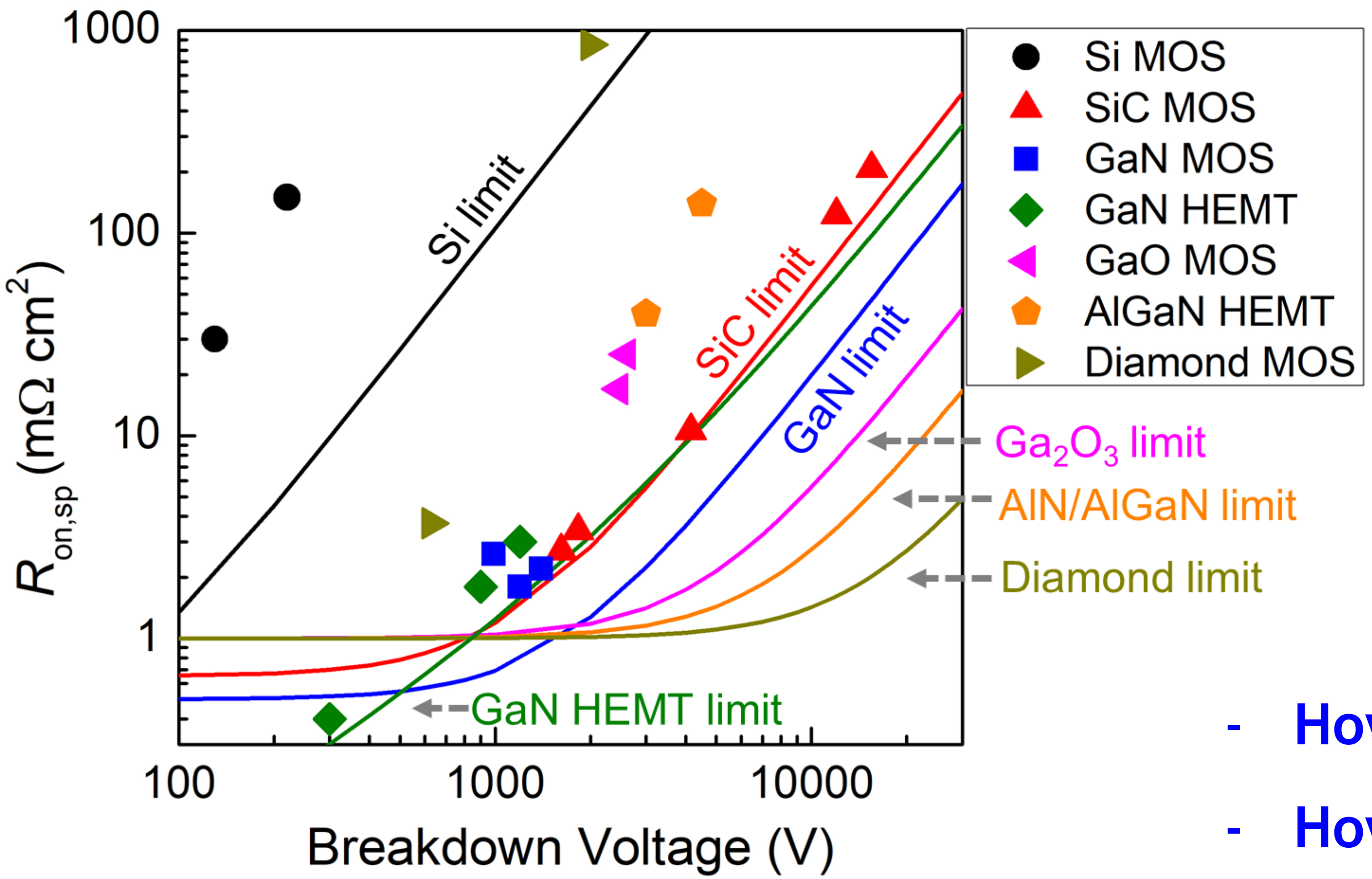
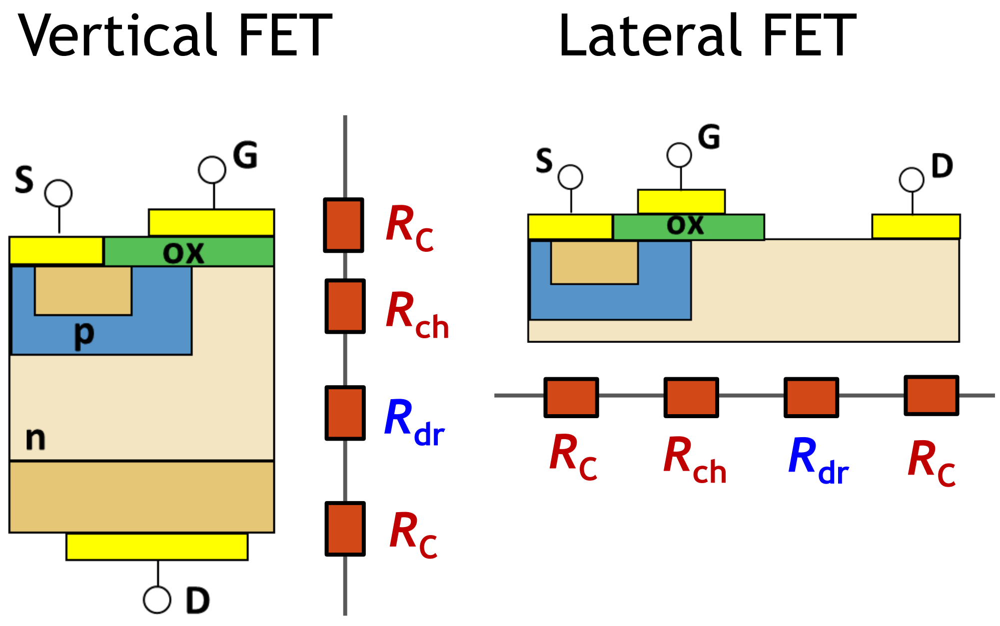
True material limits of power transistors



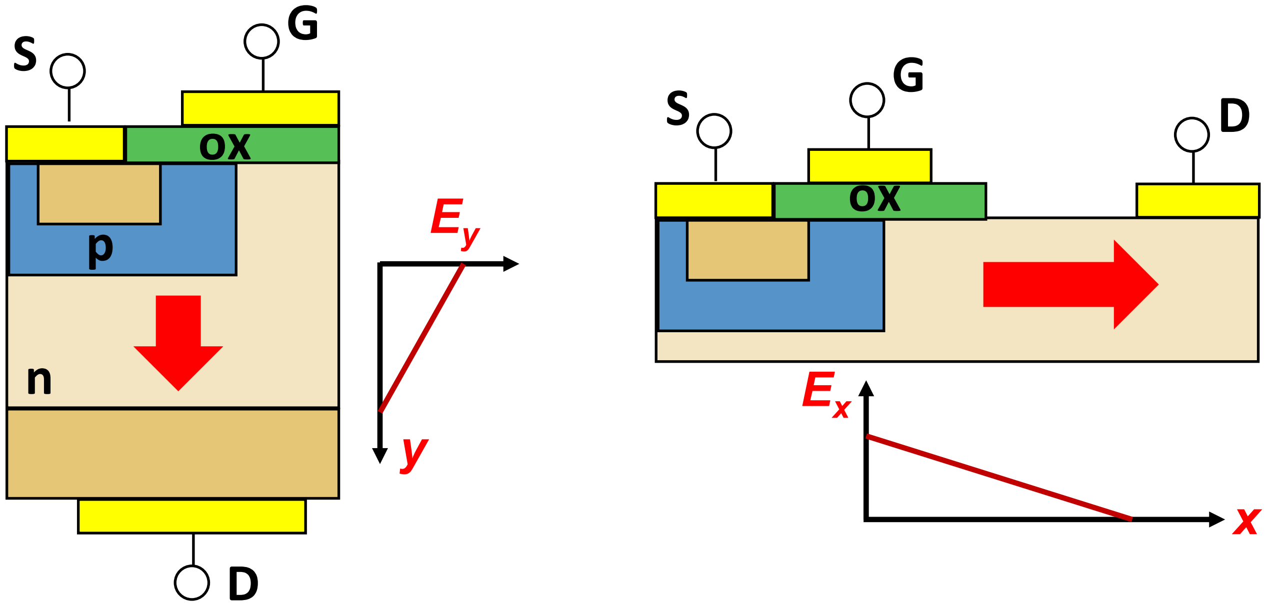


- How to slash R_C + R_{CH}? (LV)
- How to reach/break material limit? (HV)

Device architecture matters!

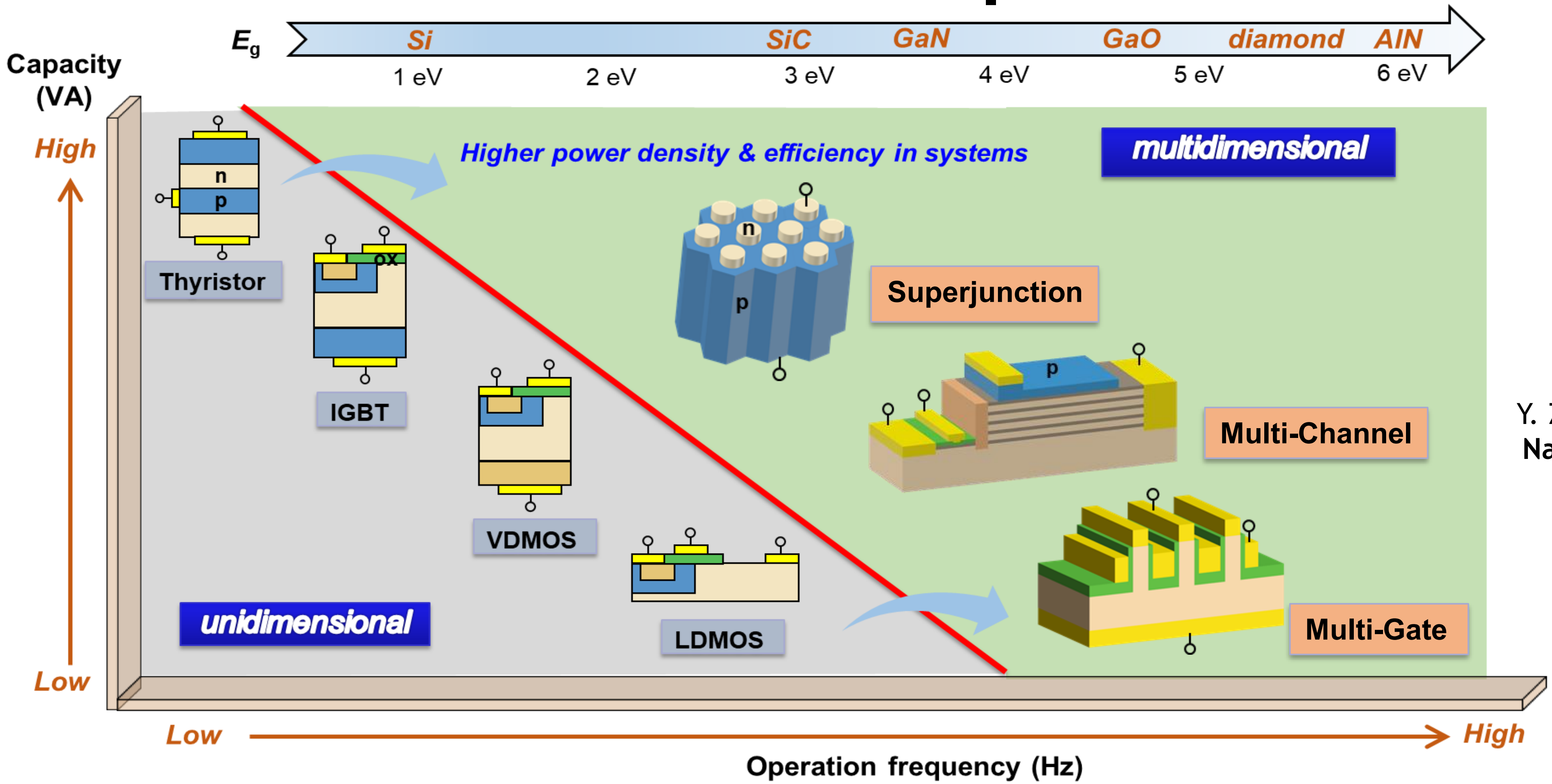
Y. Zhang, F. Udrea, H. Wang, **Nature Electronics**, 5, 723, Nov. 2022

Conventional power devices: 1D



- 1-D power device: voltage (field) blocking along the direction of current conduction

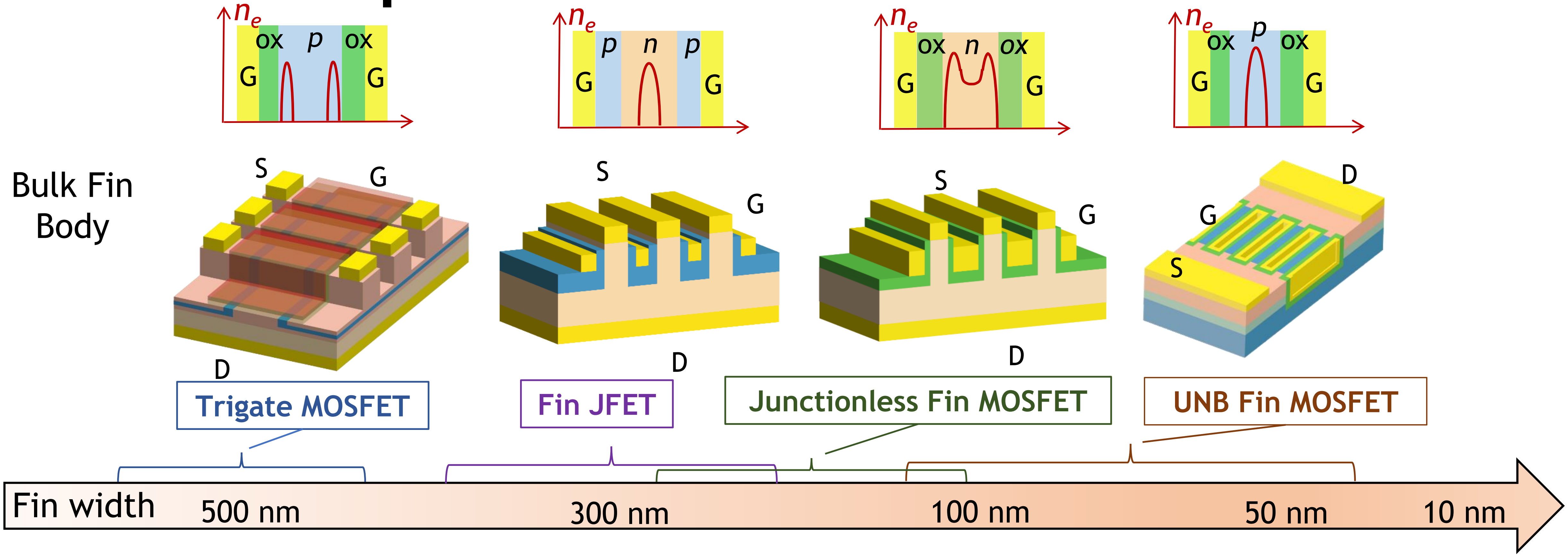
Multidimensional power devices



Y. Zhang, F. Udrea, H. Wang, **Nature Electronics**, 5, 723, Nov. 2022

- electrostatic engineering in at least one additional geometrical dimension
- break the capacity-frequency and $R_{ON,SP}$~BV trade-off

FinFET in power devices: channel innovation



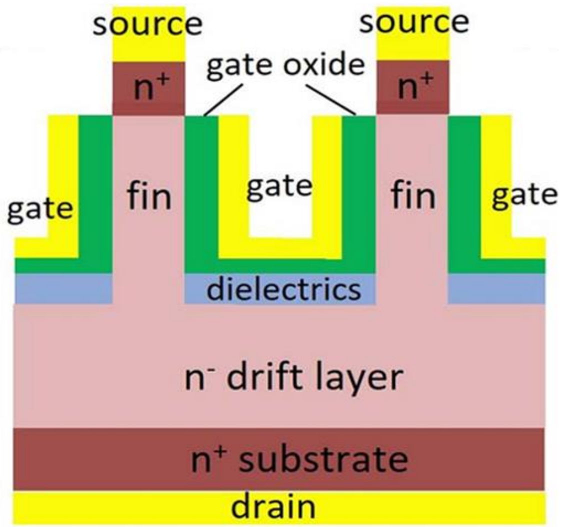
FinFET in **power**: 1) increase channel density; 2) shift carrier to high-mobility Ch.; 3) E-mode

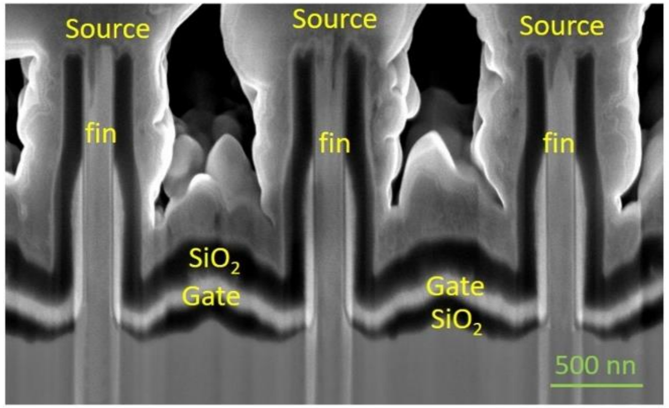
FinFET in **digital**: 1) Low SS; 2) device compactness; 3) reduce short-channel effect

Y. Zhang, F. Udrea, H. Wang, **Nature Electronics**, 5, 723, Nov. 2022

Vertical GaN FinFET: from concept to commercialization

- 1.2 kV Fin-MOSFET with 200nm-wide fins
- V_{th}~1 V; $R_{on,sp}$= 1 mΩ·cm²
- 2-inch GaN-on-GaN wafer process
- Superior $R_{ON}(Q_{OSS}+Q_{rr})$ than SiC



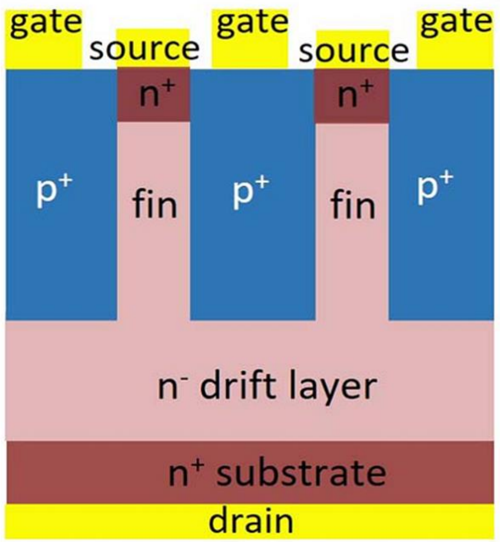


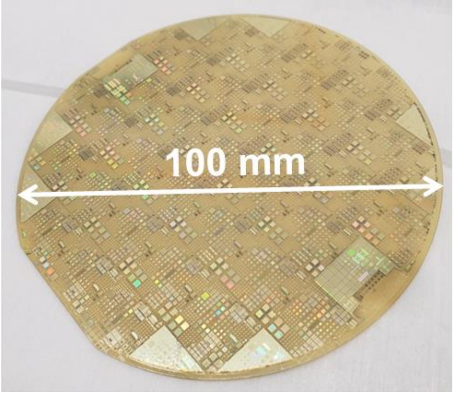
Massachusetts Institute of Technology

Y. Zhang *et al.*, **IEDM** 2017

Y. Zhang *et al.*, 40 (1), **EDL**, 2019
(2019 IEEE EDS George Smith Award)

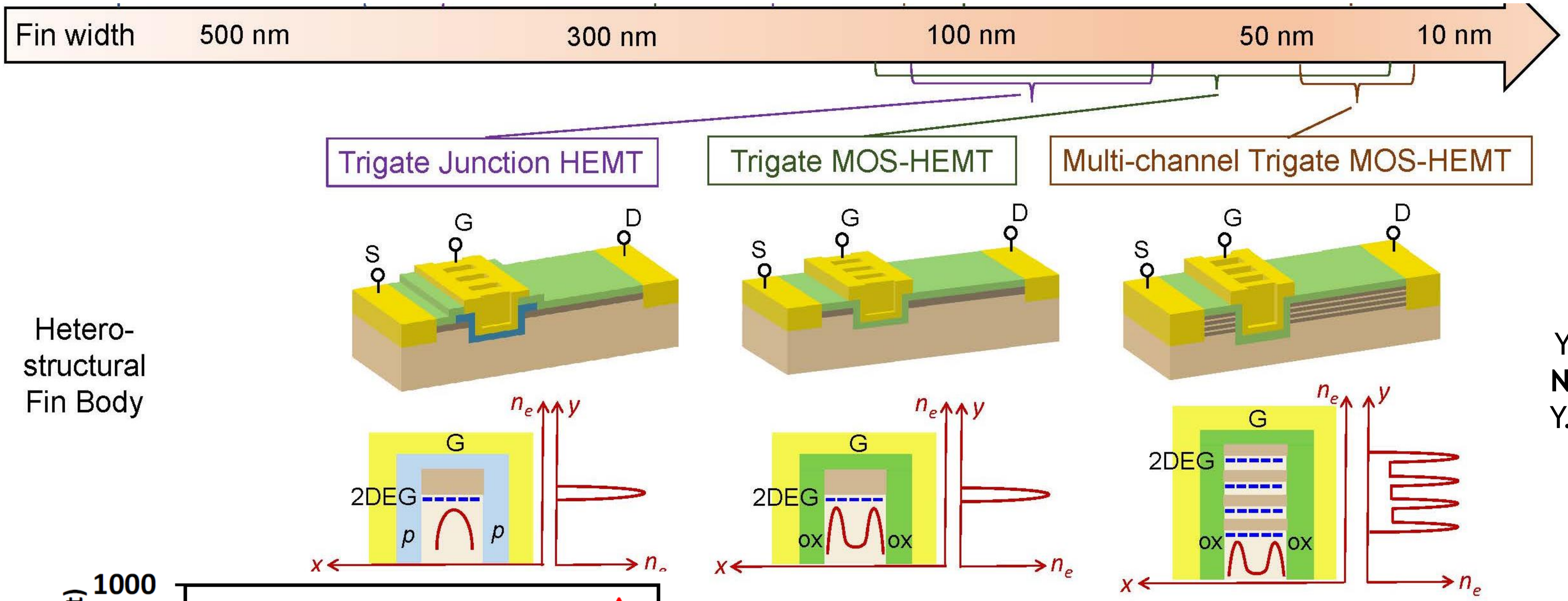
- NexGen's 1.2 kV Fin-JFET commercialization (VT characterization & application)
- $100M+ GaN-on-GaN Fab in Syracuse, NY
- 1470 V BV_{AVA}, avalanche capability, 0.82 mΩ·cm² (4-5x lower than 1.2 kV SiC MOS)



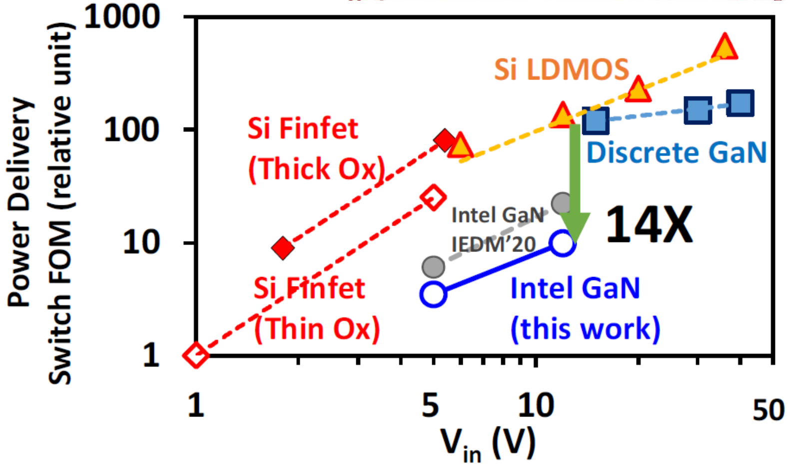


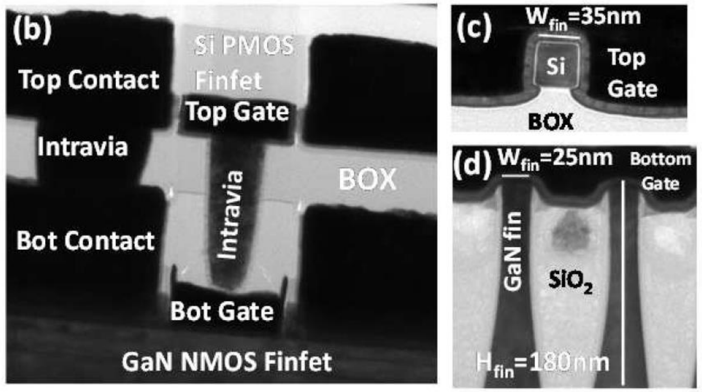
J. Liu *et al.*, **IEDM**, 23.2, 2020;
T-ED, 68, 2025, 2021

Lateral GaN Fin-HEMTs: pushing the limit of scaling and integration



Y. Zhang, F. Udrea, H. Wang, **Nat. Electron.**, 5, 723, 2022; Y. Ma *et al.*, **APL** 2020, **ISPSD** 2021, **T-ED** 2021.

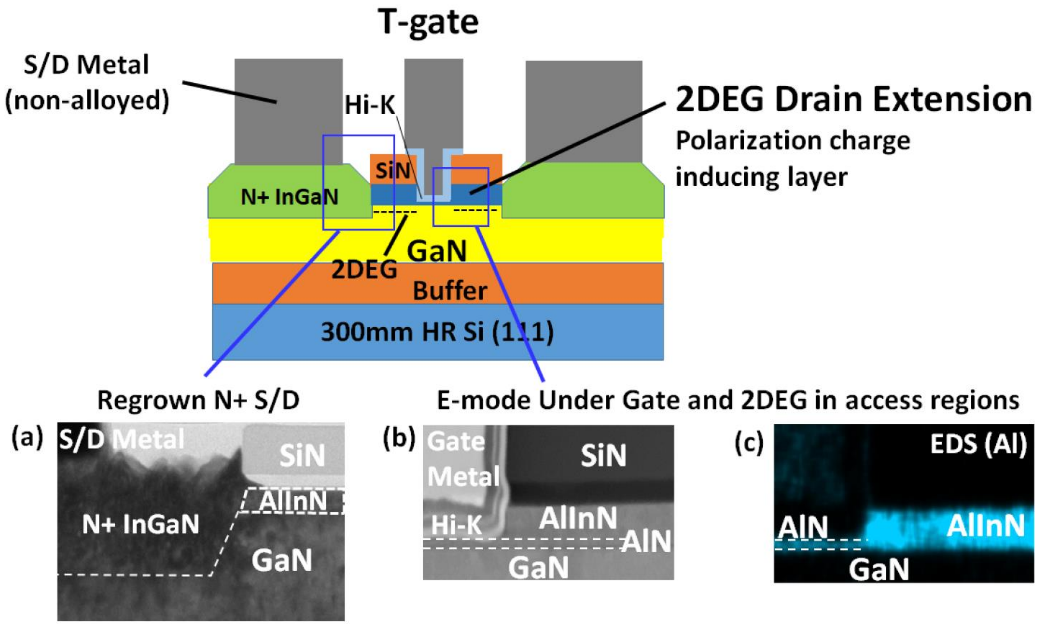


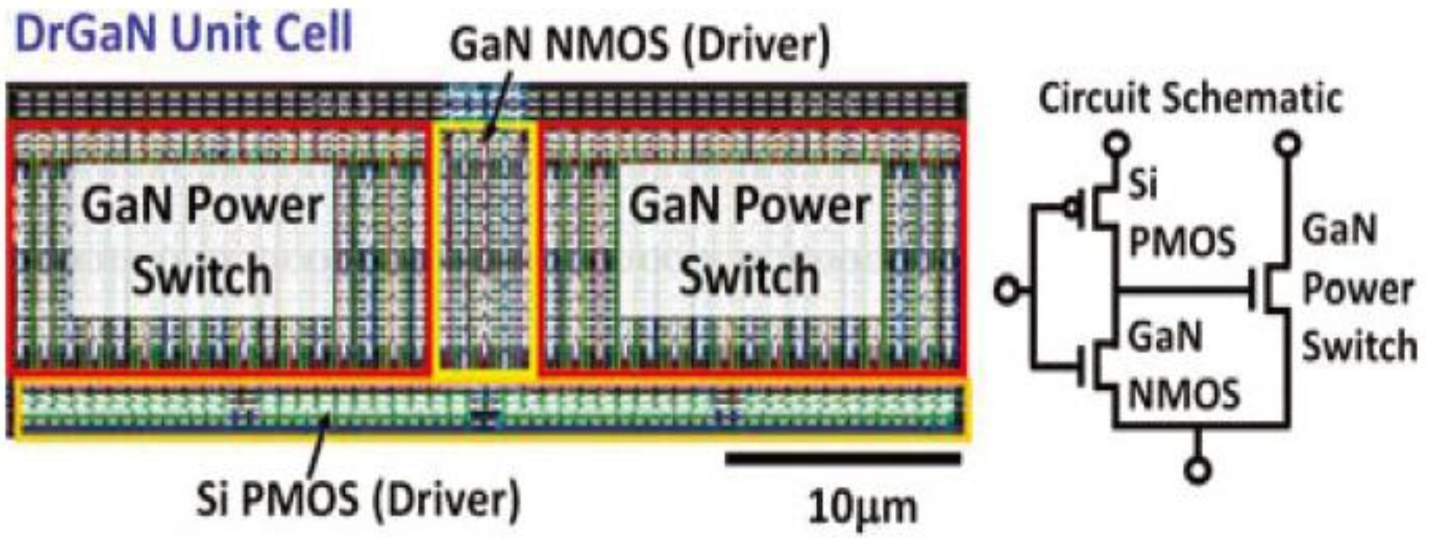


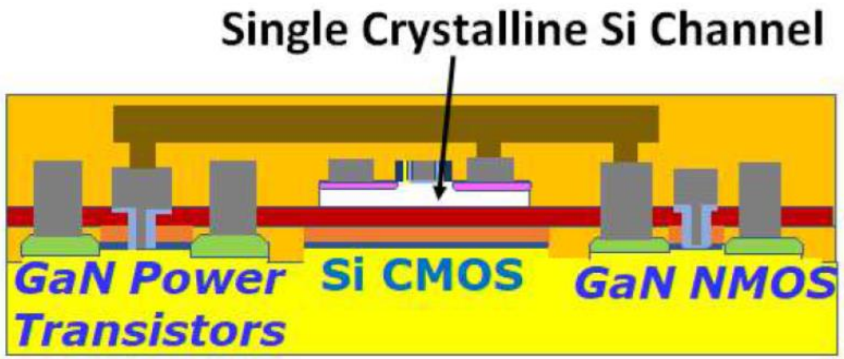
- Intel's scaled HEMT pushing GaN towards low-voltage applications
- GaN n-HEMT FinFET (power & nMOS)

Han Hui Then *et al.*, **IEDM** 21

Intel's DrGaN



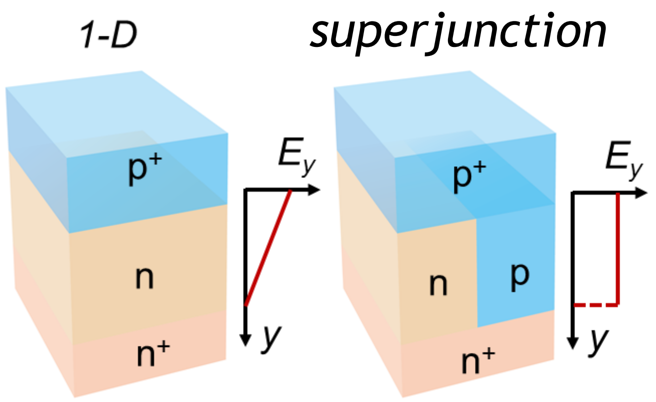


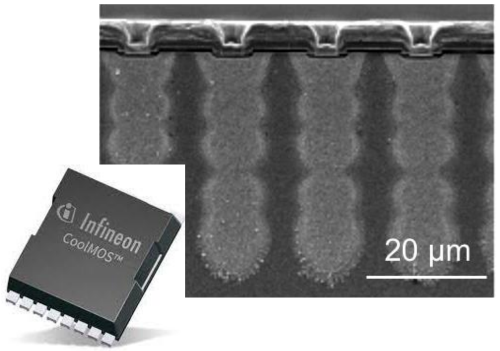


- Gate recess + regrown contact for E-mode LV HEMT
- DrGaN: GaN power switch (GaN NMOS) + GaN-Si hybrid CMOS (GaN NMOS + Si PMOS)
- Gate-last 3D monolithic integration of GaN + CMOS

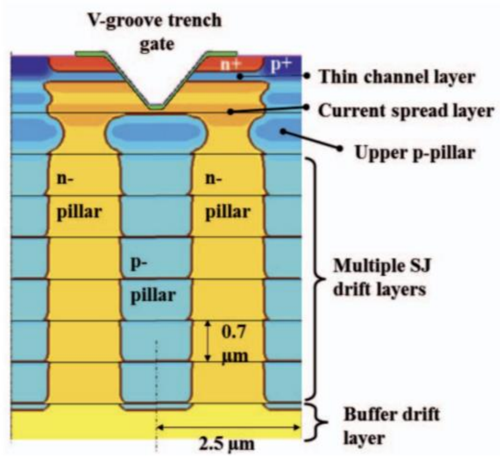
Han Hui Then *et al.*, **IEDM** 23

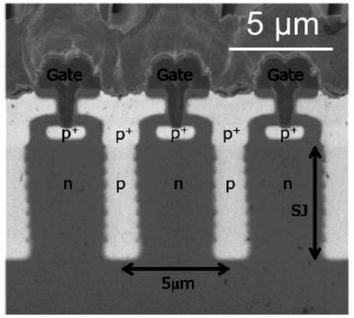
Vertical superjunction: from Si to WBG and UWBG



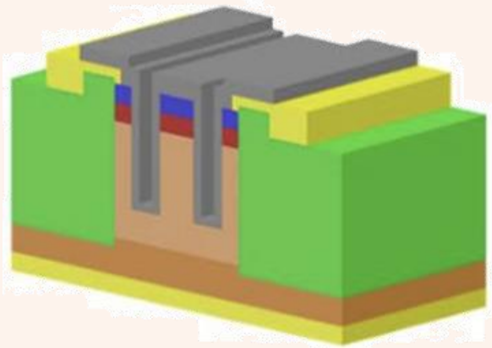


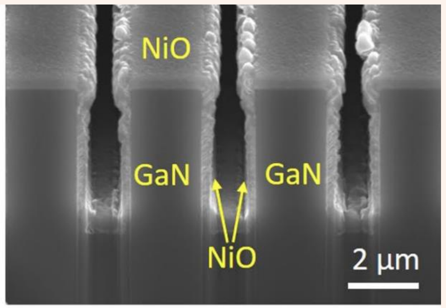
Si superjuction
commercial since 1998
~$1billion market



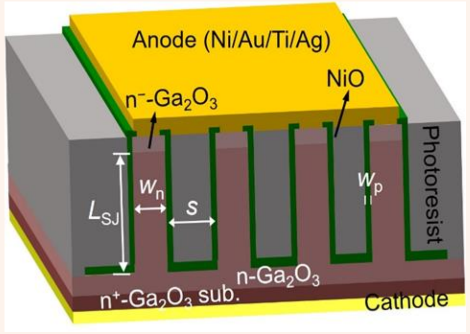


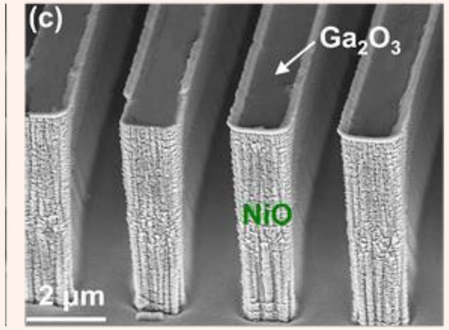
SiC superjuction
1st demo in 2016-2018
1.2kV, 0.63mΩ·cm²





GaN superjuction
1st demo (IEDM2022)
1.1kV, 0.3mΩ·cm²

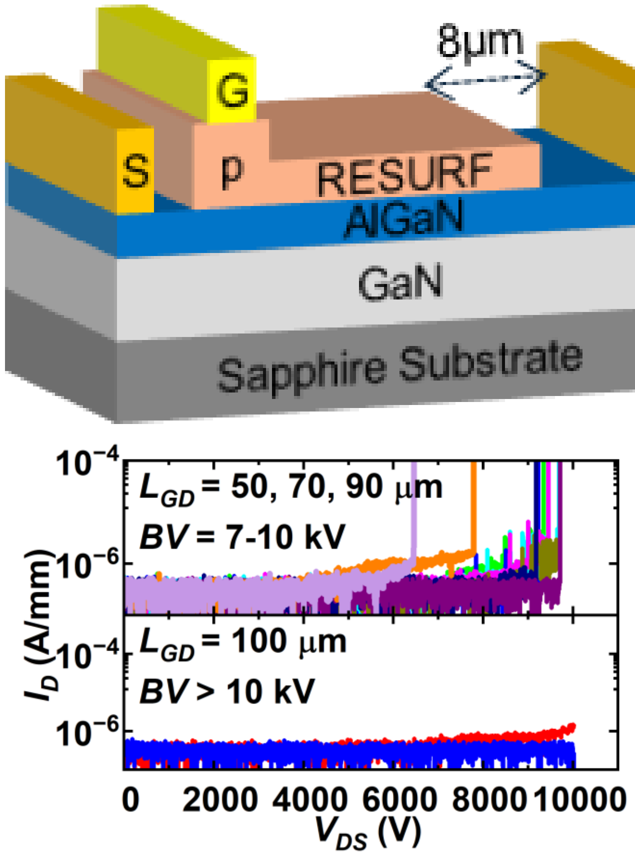


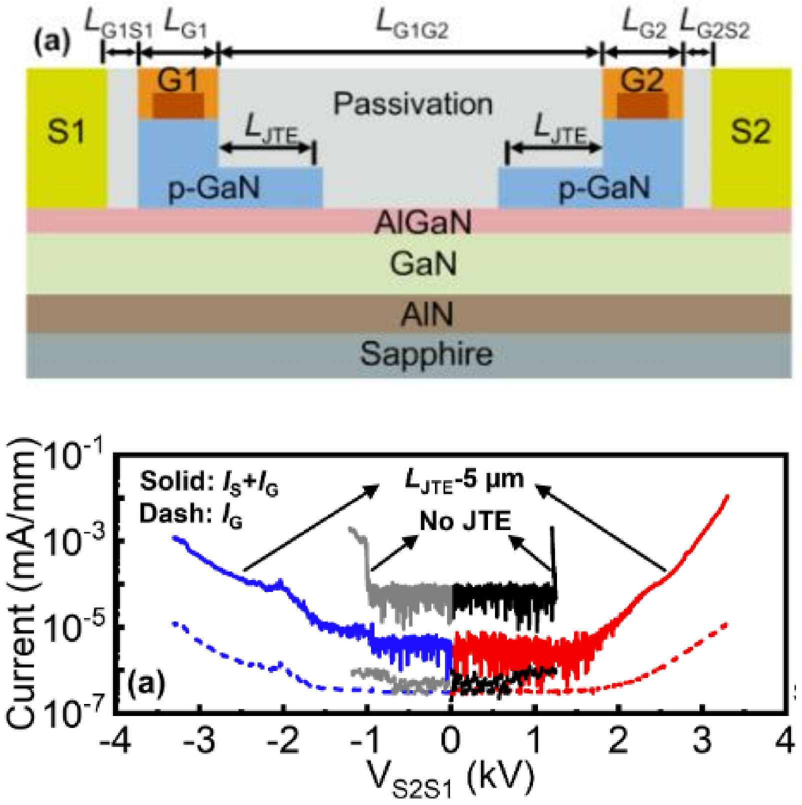


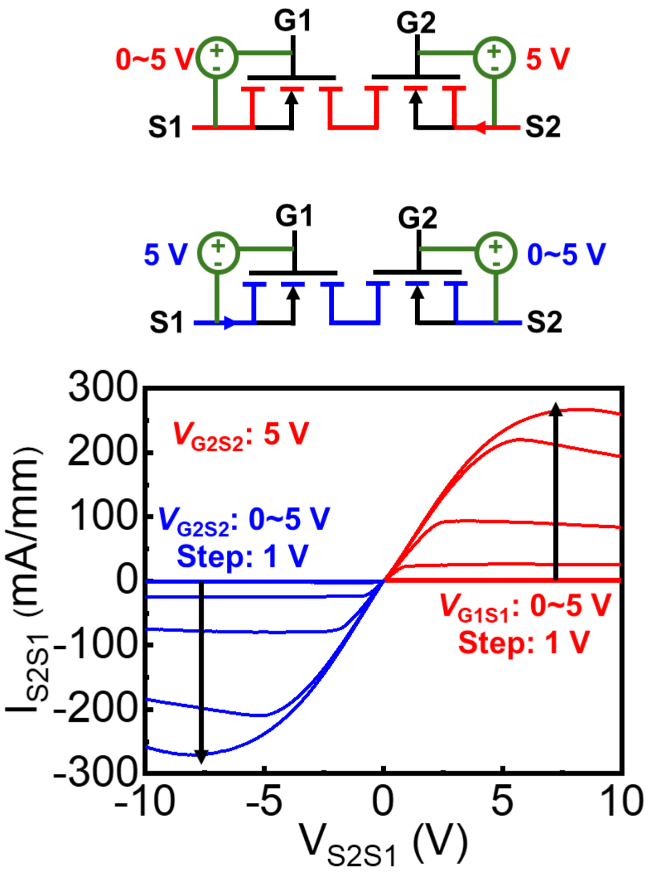
Ga_2O_3 superjuction
1st demo (IEDM2023)
2kV, 0.7mΩ·cm²

[1[T. Masuda et al., "0.63 mΩ·cm², 1170 V 4H-SiC Super Junction V-Groove Trench MOSFETM," IEDM, 2018. [2] M. Xiao *et al.*, "First demonstration of vertical sueprjunction diode in GaN", IEDM, 2022. [3] Y. Qin *et al.*, "2 kV, 0.7 mΩ·cm² vertical Ga_2O_3 superjunction Schottky rectifier with dynamic robustness," IEDM 2023.

10 kV GaN superjunction HEMT and 3.3 kV MBDS







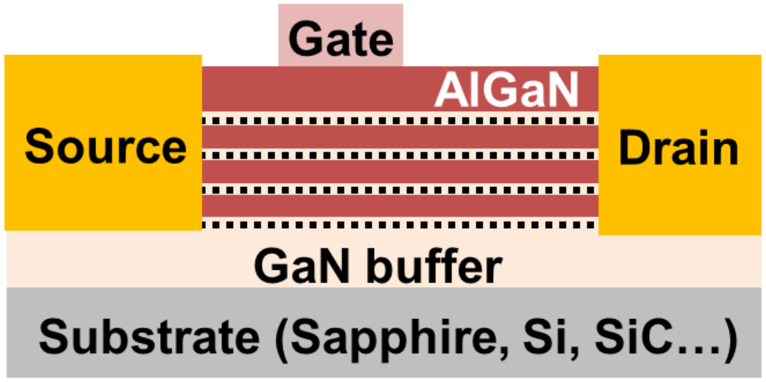
- BV upscaling enabled by charge-balance between p-GaN and AlGaN/GaN
- 10 kV, 70 mΩ·cm^2 E-mode GaN HEMT

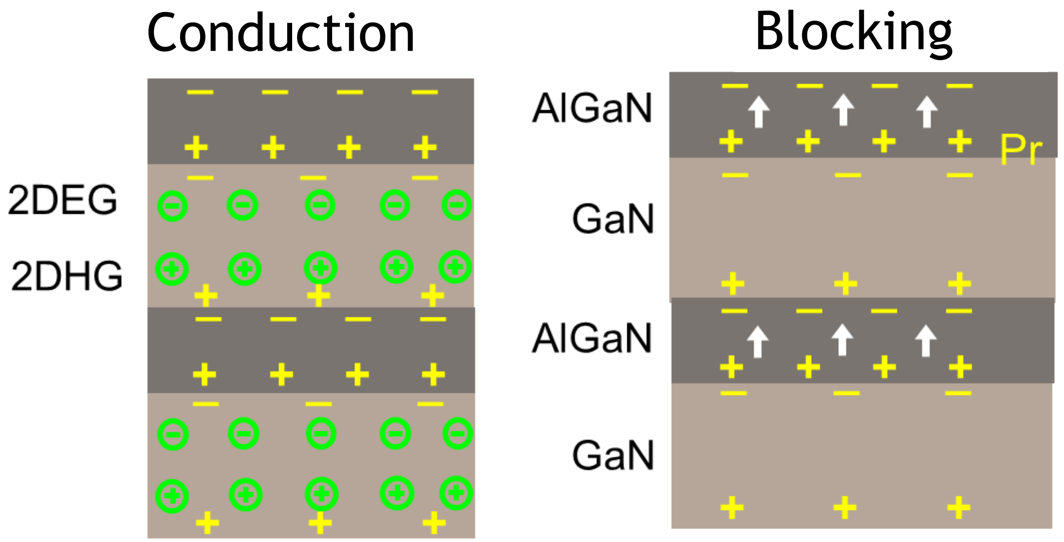
Y. Guo *et al.*, under review

- Dual p-GaN JFET improves E-field management
- 3.3 kV, 5.6 mΩ·cm^2 E-mode GaN monolithic bidirectional HEMT

Y. Guo *et al.*, EDL 2025

Multi-channel: lateral polarization superjunction



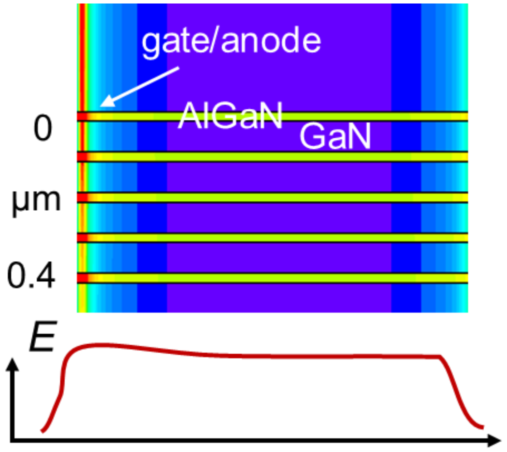


- √ High current capability
- √ Low R_{on} for HV
- √ Ideally, a natural superjunction

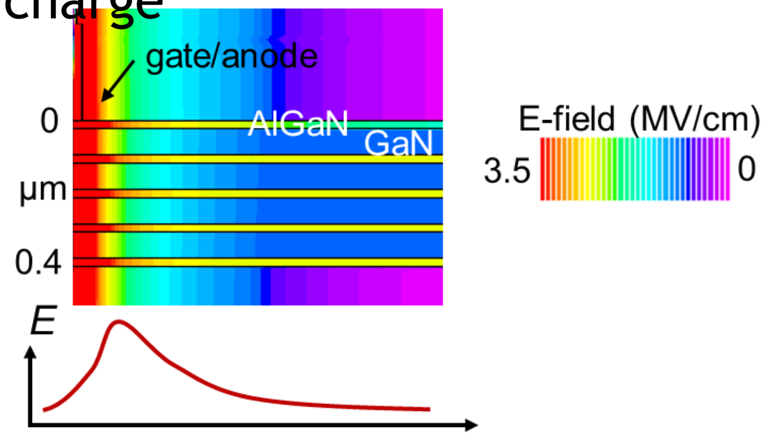
New challenges:

- **(non-ideal) E-field management**
- **E-mode gate**

Ideal multi-channel



Multi-channel w/ net charge



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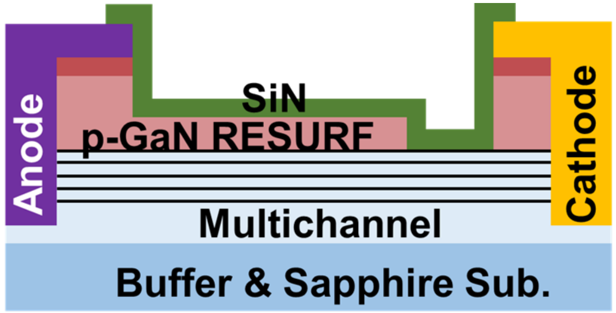
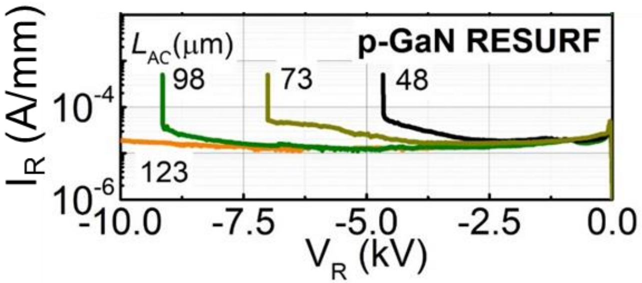
Multi-channel: 10kV GaN with $R_{ON,SP}$ 2.5x lower than SiC

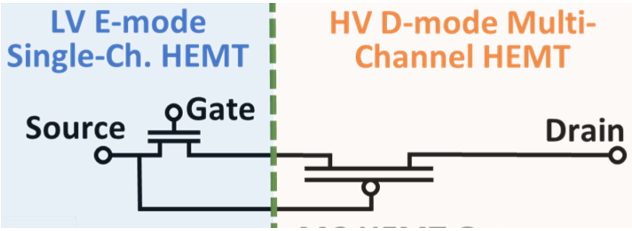
- 4-inch wafer, five channels, R_{SH} 120 Ω/sq
- p-GaN charge balance with multi-channel (superjunction design)
- *BV* > 10 kV, $R_{ON,SP}$ = 39 mΩ·cm^2

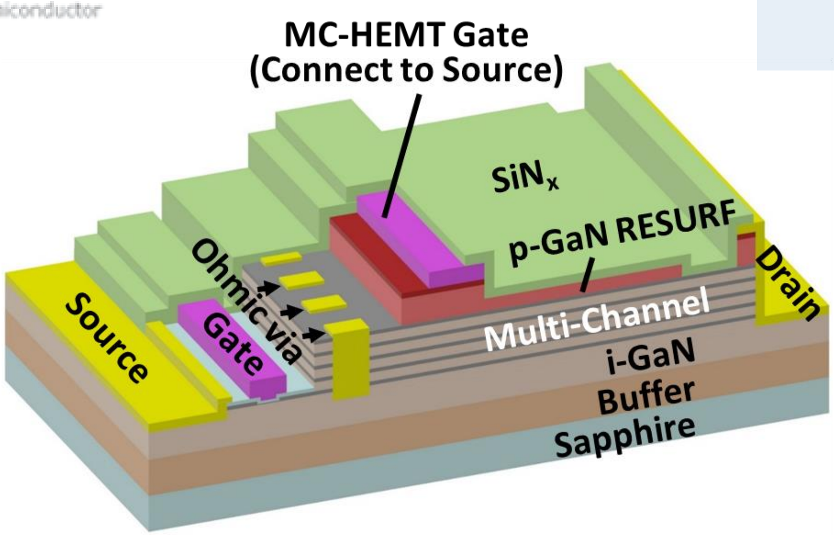


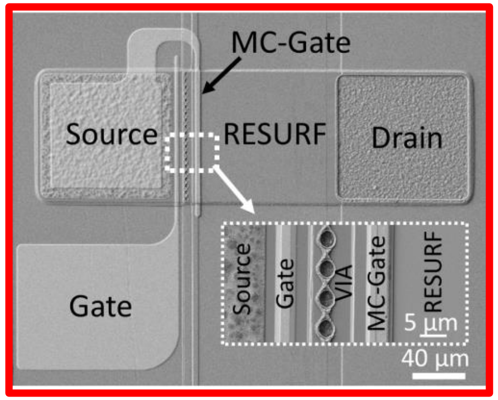


M. Xiao *et al.*, "10 kV, 39 mΩ·cm^2 Multi-channel AlGaN/GaN Schottky barrier diodes," *IEEE Electron Device Letters*, 2021.

- <u>M</u>ulti-<u>C</u>hannel <u>M</u>onolithic-<u>C</u>ascode HEMT (MC^2-HEMT)
- V_{TH} > 1.5 V; I_{SAT} > 300 mA/mm; $R_{ON,SP}$ of 40 mΩ·cm^2
- Best FOM in 6.5kV+ power transistors

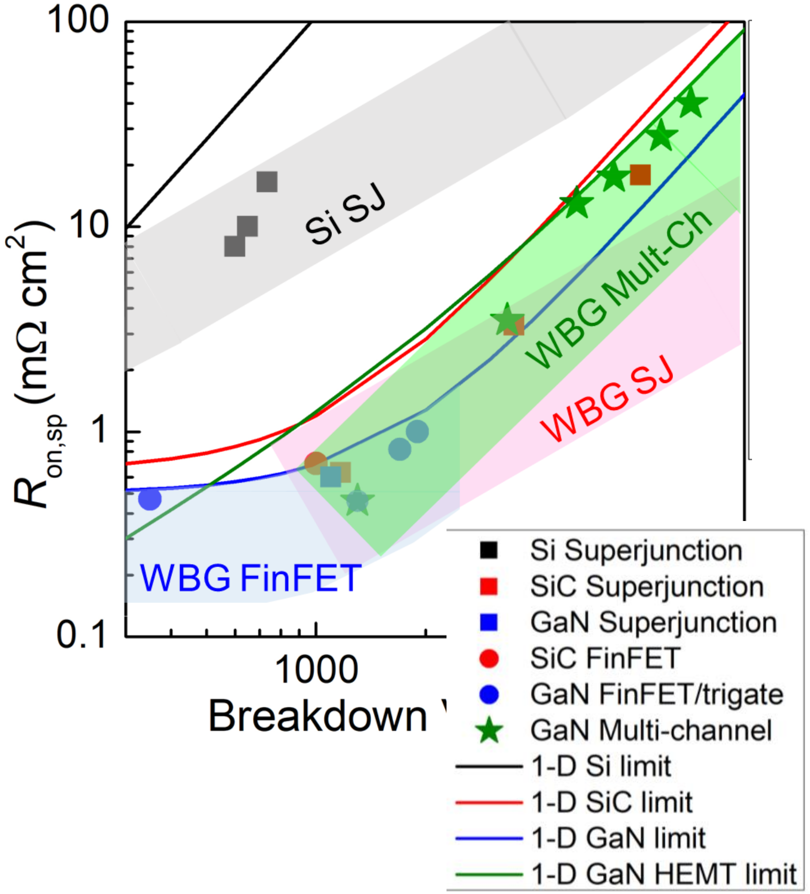


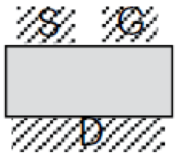
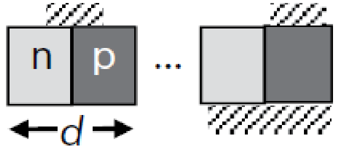
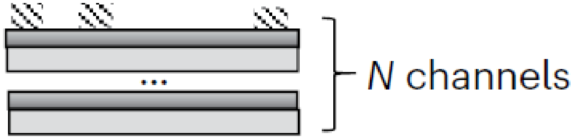




M. Xiao *et al.*, "Multi-Channel Monolithic-Cascode HEMT (MC2-HEMT): A New GaN Power Switch up to 10 kV," *IEDM*, 2021.
(IEDM Technical Highlights, Nature Electronics Coverage)

Multidimensional devices: new limits and new scaling laws



Drift region design	1D	2D superjunction	Multi-channel (PSJ)
Structure			
Performance limit	$R_{ON,SP} = \frac{4}{\varepsilon\mu E_C^3} BV^2$	$R_{ON,SP} = \frac{4d}{\varepsilon\mu E_C^2} BV$	$R_{ON,SP} = \frac{BV^2}{NqE_C^2 n_{2D} \sum_{e,h} \mu_{2D}}$
Scaling parameter	NA	Cell pitch (d)	Channel number (N)
Scaling limit	NA	$d = \frac{50E_g}{9qE_C}$	Process and technology related
Minimum specific on-resistance	$\frac{4BV^2}{\varepsilon\mu E_C^3}$	$\frac{20E_g BV}{q\varepsilon\mu E_C^3}$	–
Material FOM	$\varepsilon\mu E_C^3$	$\varepsilon\mu E_C^{2.5}$	$E_C^2 n_{2D} \sum_{e,h} \mu_{2D}$

- Performance of multidimensional devices exceed 1D SiC and GaN limits
- Allow geometrical scaling in power devices! (limit: line -> band)

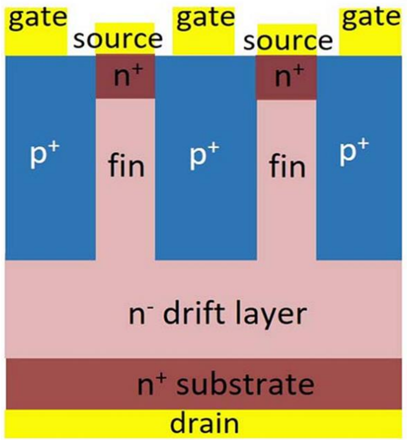
Y. Zhang, F. Udrea, H. Wang, **Nature Electronics**, 5, 723, Nov. 2022

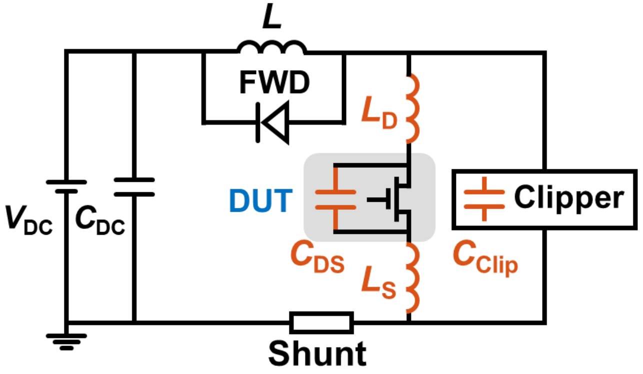
Outline

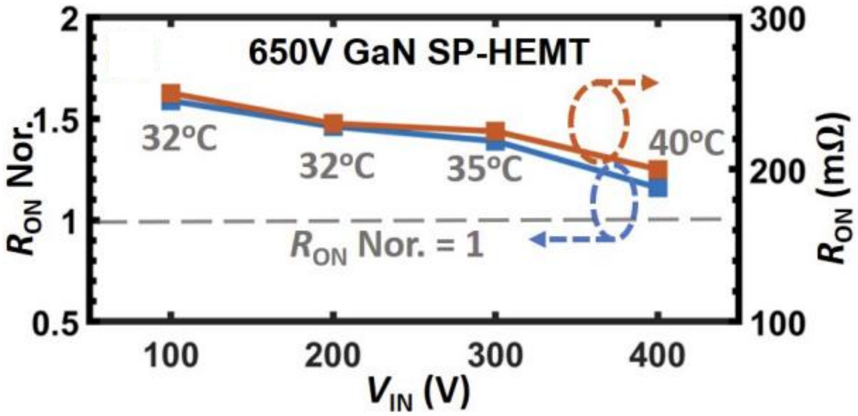
- *How to make GaN device better for LV and HV?*
  - Multidimensional architecture
  - FinFET, superjunction and multi-channel
  - New theoretical limits and scaling laws
- *What system benefits can new GaN devices enable?*
  - Dynamic R_{ON} free, avalanche and short-circuit robust
  - Kilovolt, megahertz soft switching

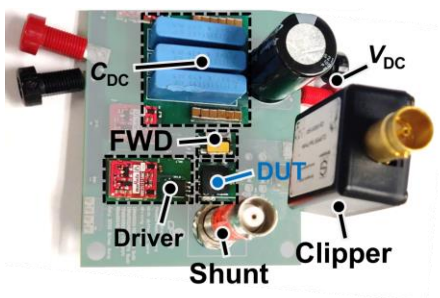
GaN devices can be dynamic Ron free

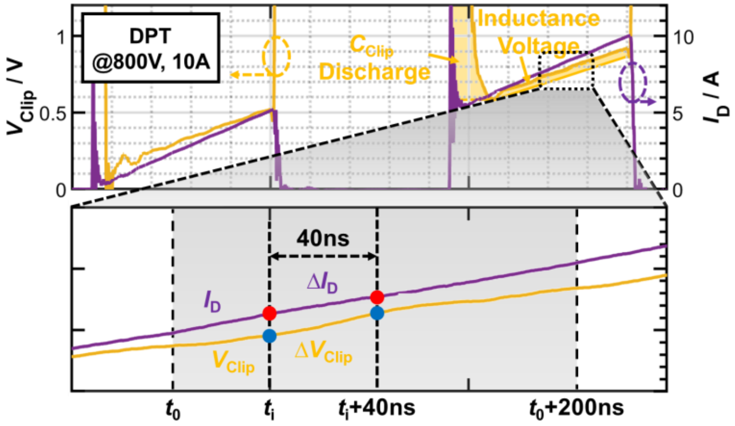
- Vertical GaN JFET are dynamic R_{ON} free under various voltage, current, temperature conditions
- Physics: 1) low dislocation density of GaN-on-GaN; 2) the absence of electric field crowding near the surface; 3) the minimal charge trapping in the native junction gate.

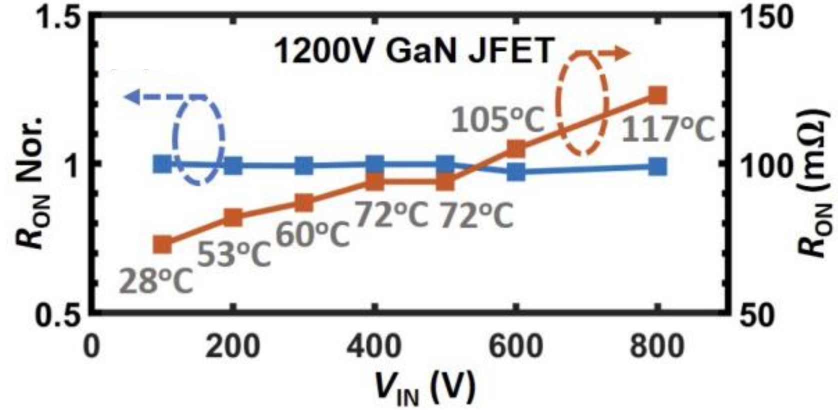








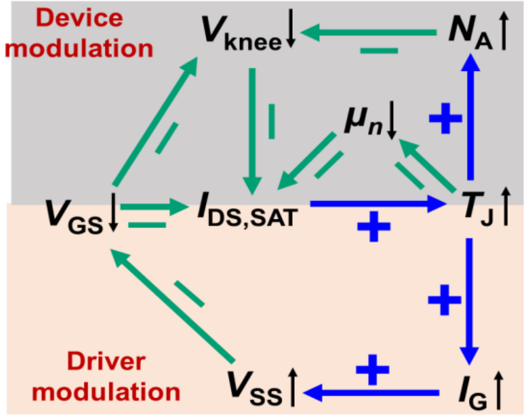


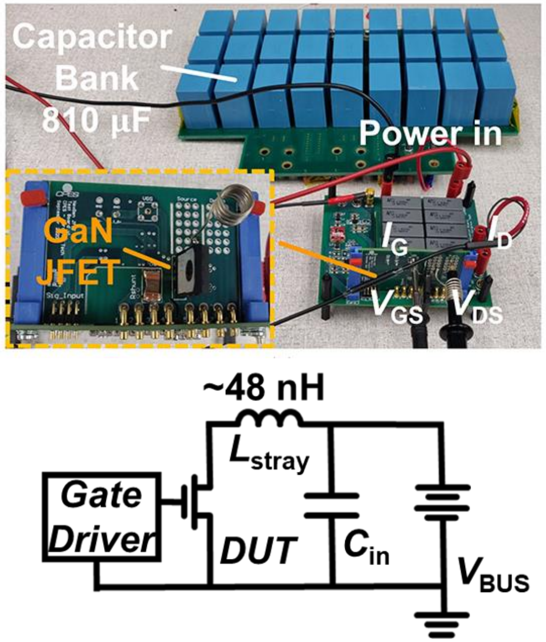


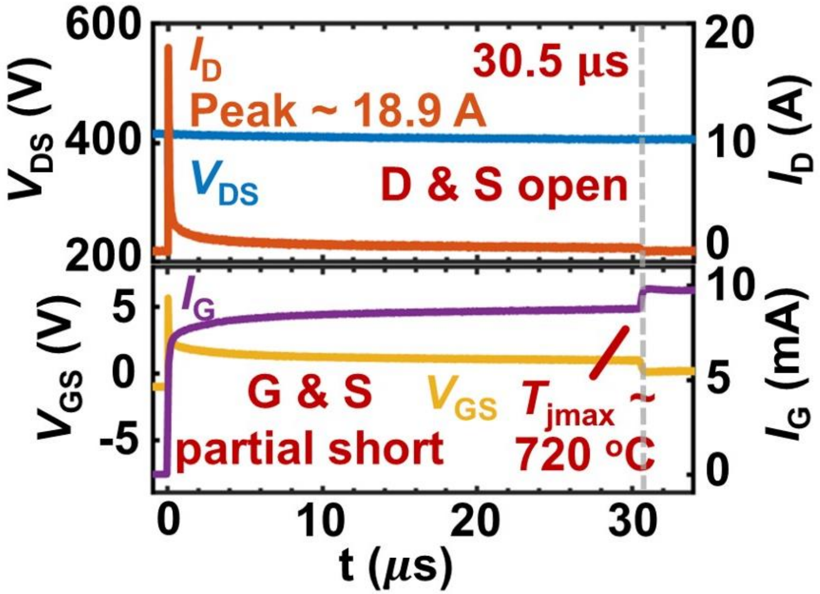
X. Yang *et al.*, "Dynamic R_{ON} Free 1.2 kV Vertical GaN JFET," IEEE Trans. Electron. Dev., 2023

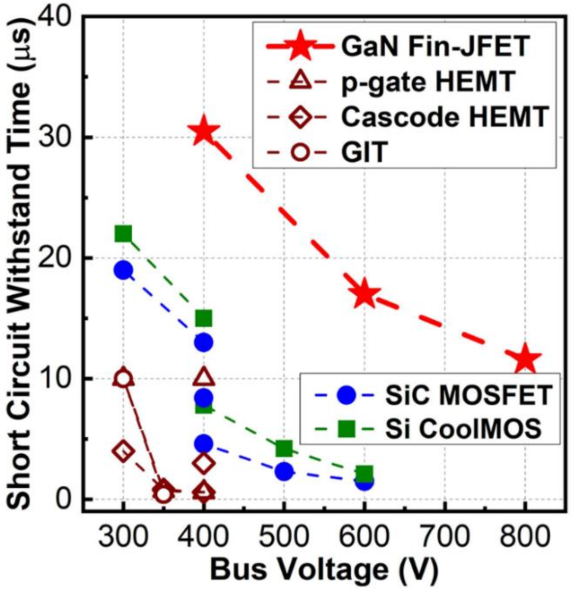
GaN devices can achieve breakthrough short-circuit robustness

- 650V GaN JFET: 30.5 μs @ 400 V, 10.6 μs @ 800 V (BV_{AVA})
- 1200V GaN JFET: >40 μs @ 800 V
- Physics: device-driver circuit interplay to suppress I_{SAT} at high temp



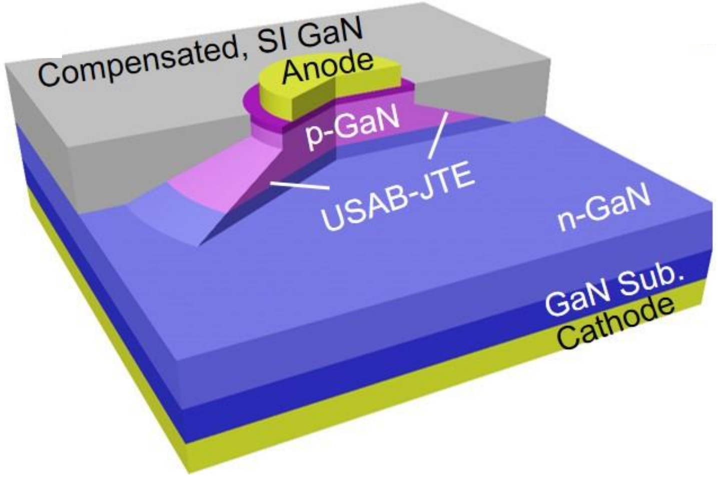


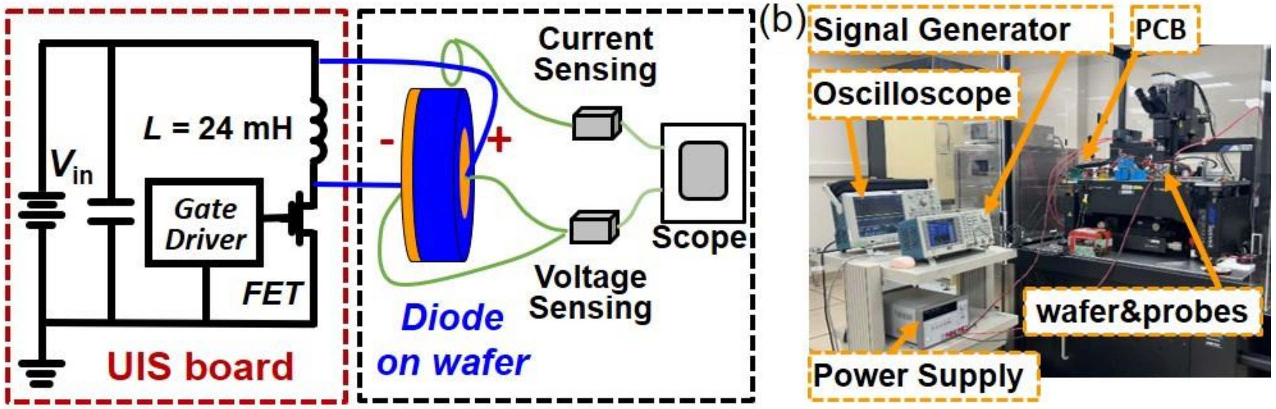


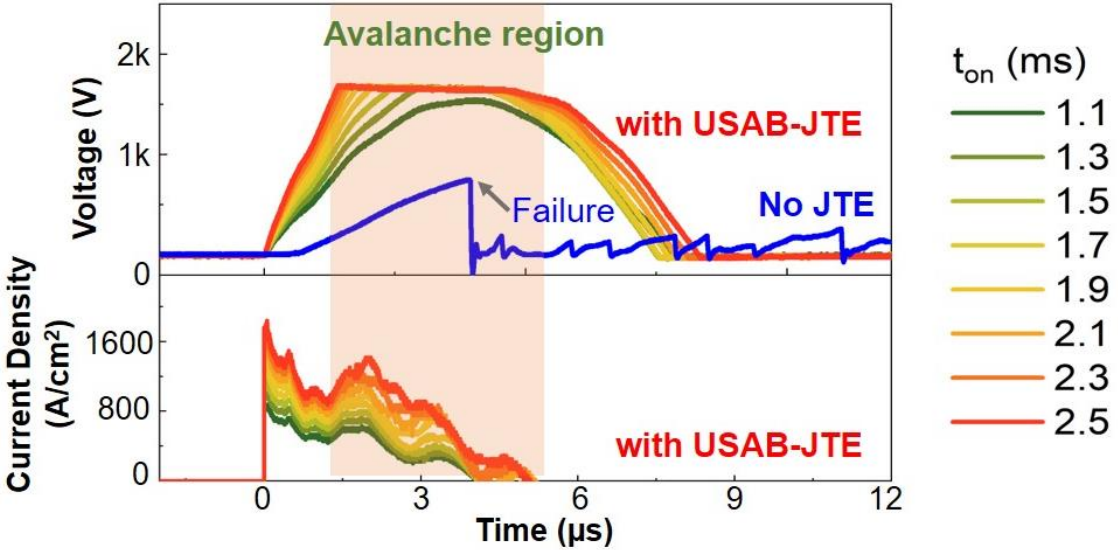


R. Zhang *et al.*, "Breakthrough short circuit robustness demonstrated in vertical GaN fin JFET," IEEE Trans. Power Electron. 2022
X. Yang *et al.*, "Evaluation and MHz Converter Application of 1.2-kV Vertical GaN JFET," IEEE Trans. Power Electron. 2024

GaN devices can have strong avalanche with right edge termination





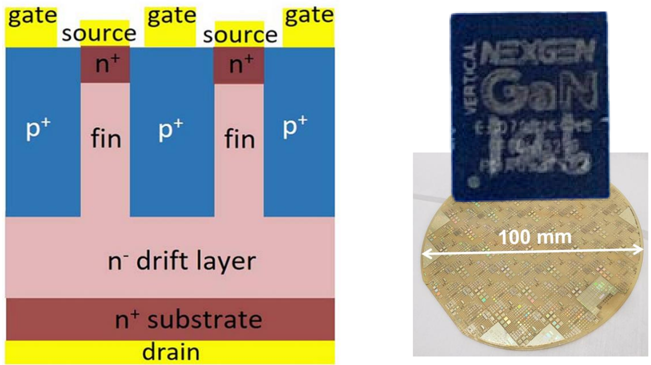


- True avalanche (high I_{AVA} @ BV_{AVA}) needs to be validated by avalanche circuit test
- Enabling structure: small-angle beveled junction termination extension (JTE)
- Fabricated by a single implantation into p-GaN using beveled PR or dielectric mask

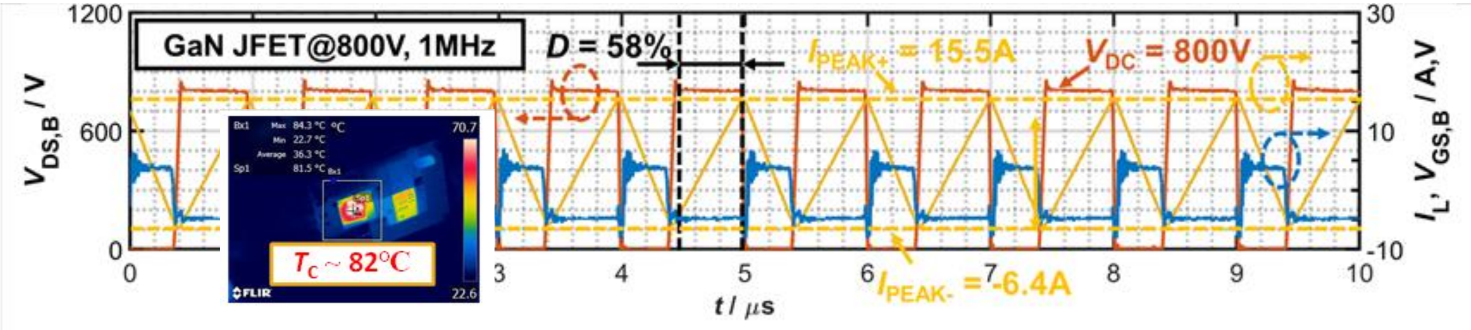
M. Xiao *et al.*, "Robust avalanche in 1.7 kV vertical GaN diodes with a single-implant bevel edge termination," EDL, (**IEEE George Smith Award 2023**)

GaN power FinFET enables kilovolt, MHz applications

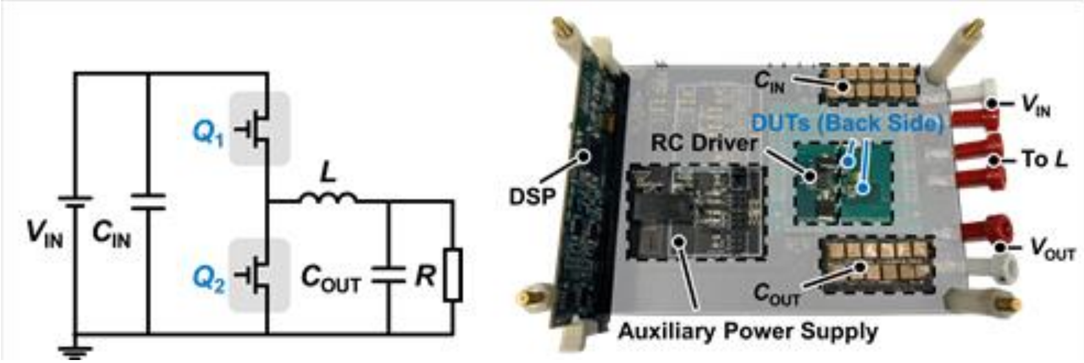
1.2kV,70mΩ GaN FinFET in DFN package



800V, 1MHz switching with wide D range



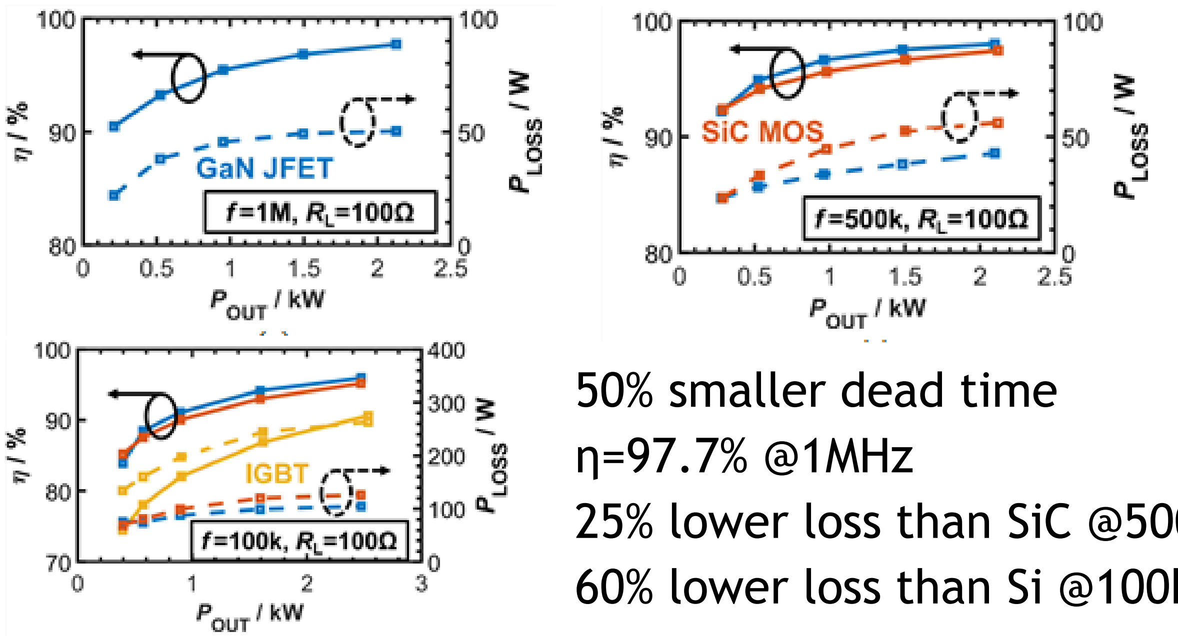
Zero-voltage-switching buck converter



- turn-on loss >> turn-off loss
- zero dynamic R_{ON}

X. Yang *et al.*, "Evaluation and MHz Converter Application of 1.2-kV Vertical GaN JFET," **T-PEL** 2024

Higher *f* and efficiency than SiC and Si FETs



50% smaller dead time
η=97.7% @1MHz
25% lower loss than SiC @500kHz
60% lower loss than Si @100kHz

Summary

- Plenty of room for GaN at the top and bottom
  - Huge market opportunities
  - GaN offers superior FOM and lower cost; unique advantages in integration
- But GaN device requires innovation for emerging LV and HV applications
- Multidimensional structures have enabled superior FOMs; geometrical scaling can break the conventional limits
  - **FinFET and trigate**: lower the channel resistance; initial industry adoptions; can be key building blocks for both LV and HV devices
  - **Superjunction**: charge balance enables BV upscaling in GaN devices
  - **Multi-channel**: a new platform for HV lateral devices up to 10 kV
- Initial circuit applications and superior reliability
  - GaN device can be dynamic R_{ON} free, avalanche and short-circuit robust
  - Kilovolt, MHz converter, outperforming SiC and Si in converters