Application-Oriented Stability, Reliability, and Robustness of GaN Power Devices

Yuhao Zhang, Professor, University of Hong Kong
Email: yuhzhang@hku.hk

2025/08/14

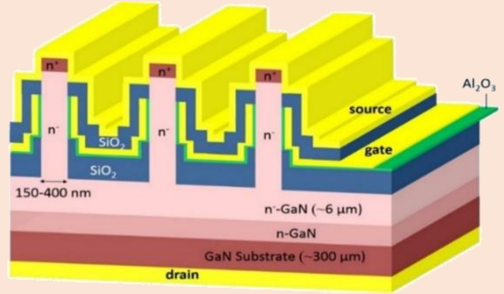
Research scope of my group

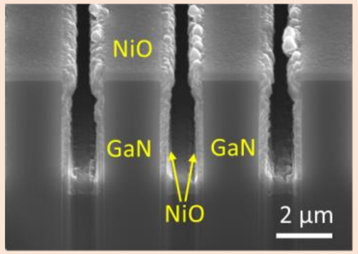
Performance, Reliability, Cost

Sciences → **Applications**

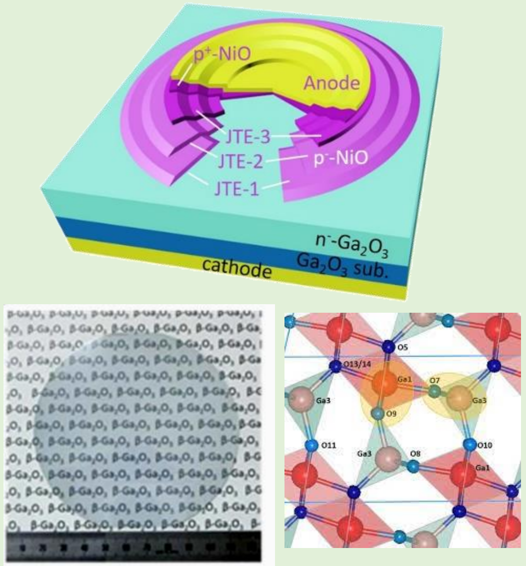
Physics & Material	Device Design	Processing Technologies	Device Charact. and Application	Robustness & Reliability	Packaging	Converter

Multidimensional Device Architectures

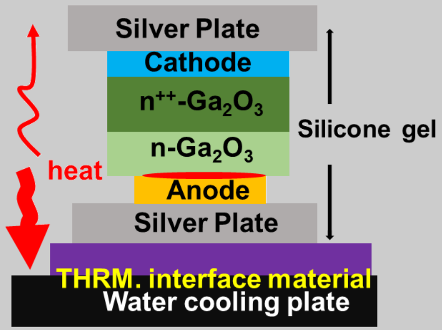


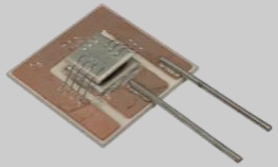


(Ultra) Wide Bandgap Materials

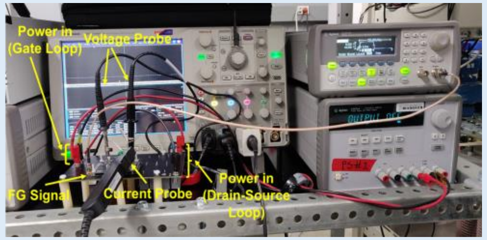


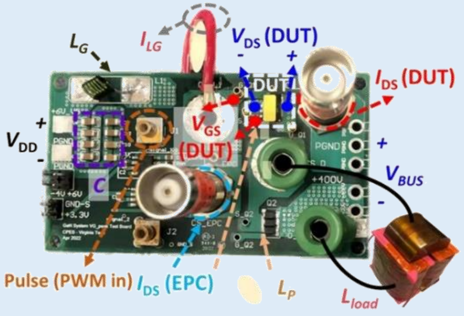
Packaging & Thermal Management





Circuit-based Reliability & Application





we work on Si IGBT, SiC MOSFET, GaN HEMT, Ga_2O_3 devices…

Power semiconductors as pathways to carbon neutrality

nature reviews electrical engineering

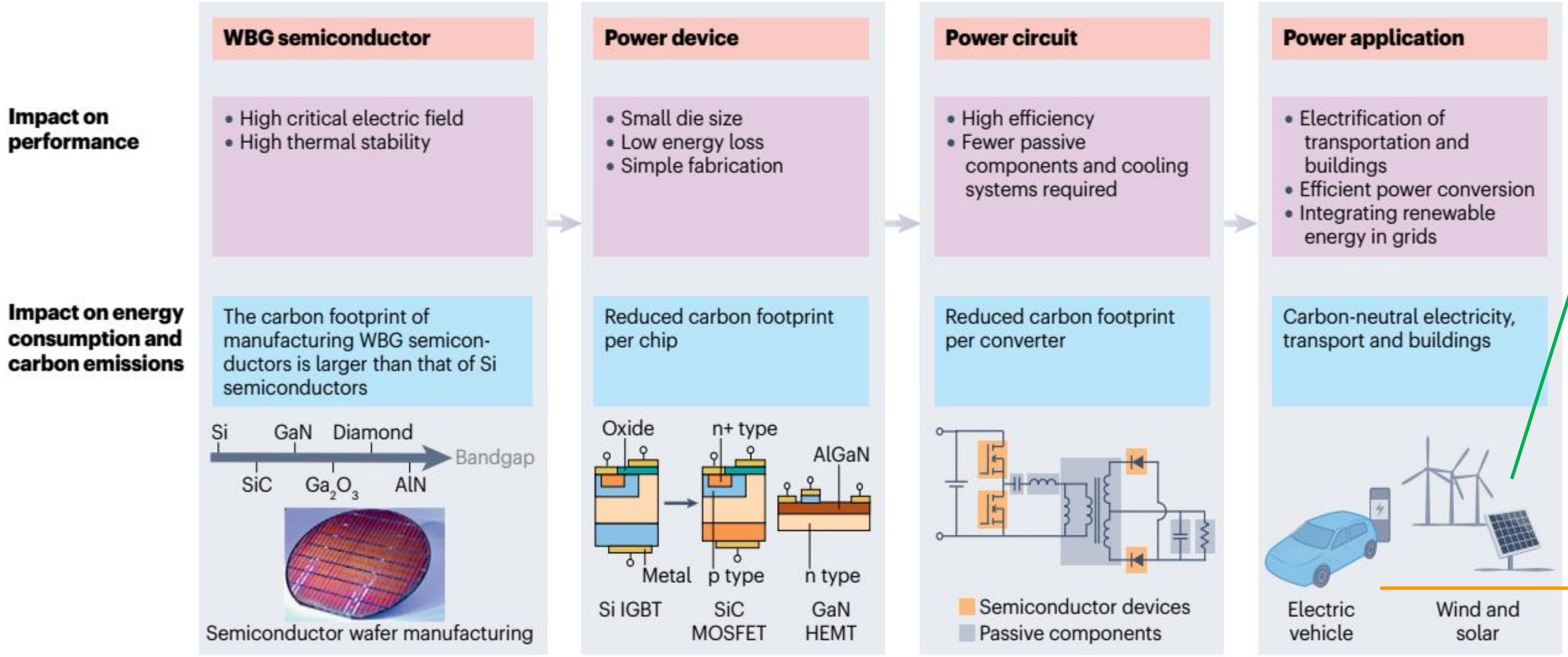
Review Article | Published: 21 January 2025

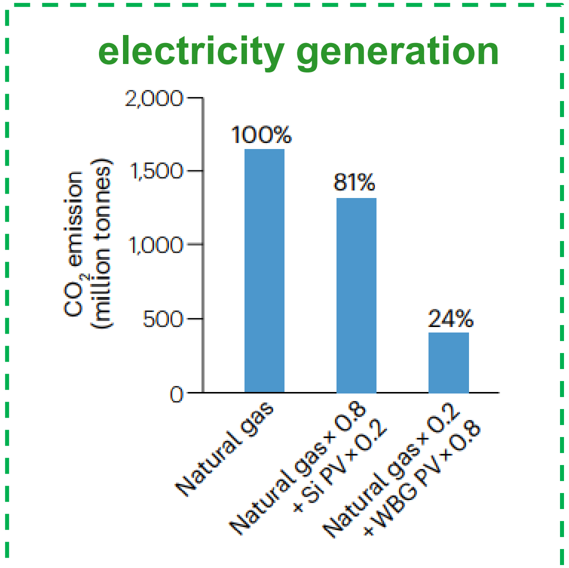
Wide-bandgap semiconductors and power electronics as pathways to carbon neutrality

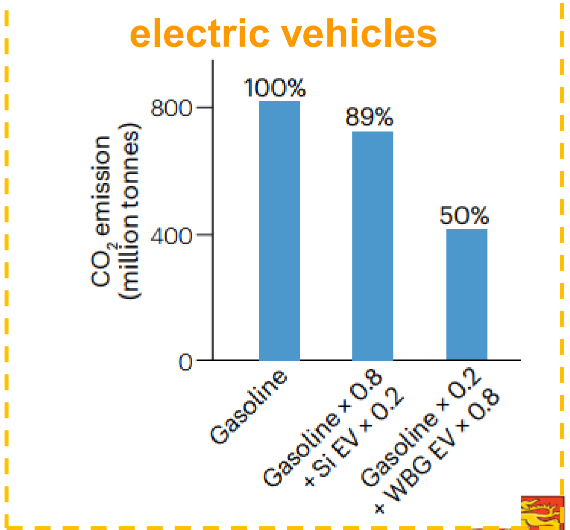
Yuhao Zhang, Dong Dong, Qiang Li, Richard Zhang, Florin Udrea & Han Wang

Nature Reviews Electrical Engineering **2**, 155–172 (2025) | Cite this article

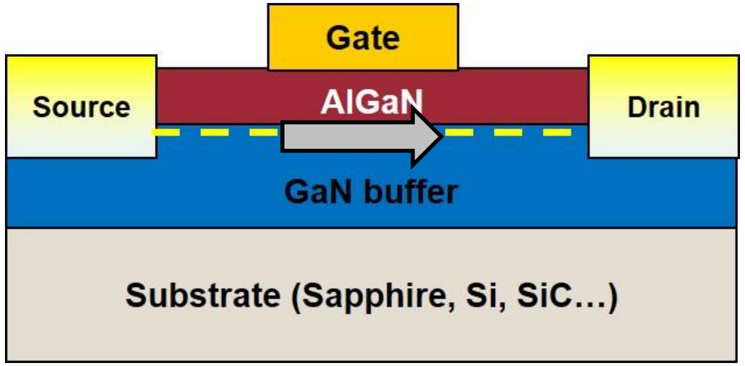
WGB replacing Si can enable an annual carbon saving of at least 20 million tonnes in the USA – annual emissions of 4 million gasoline passenger vehicles



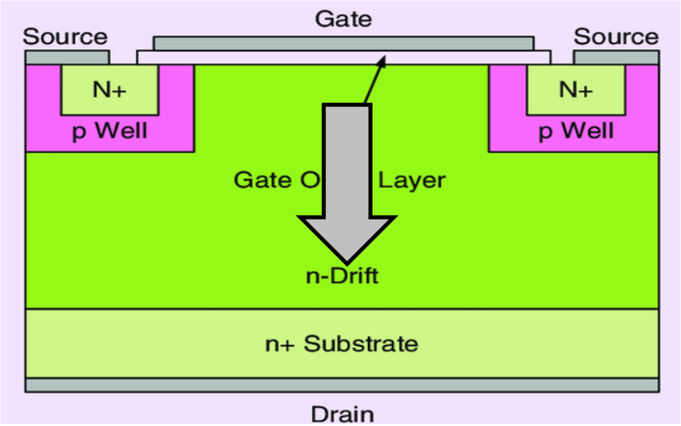




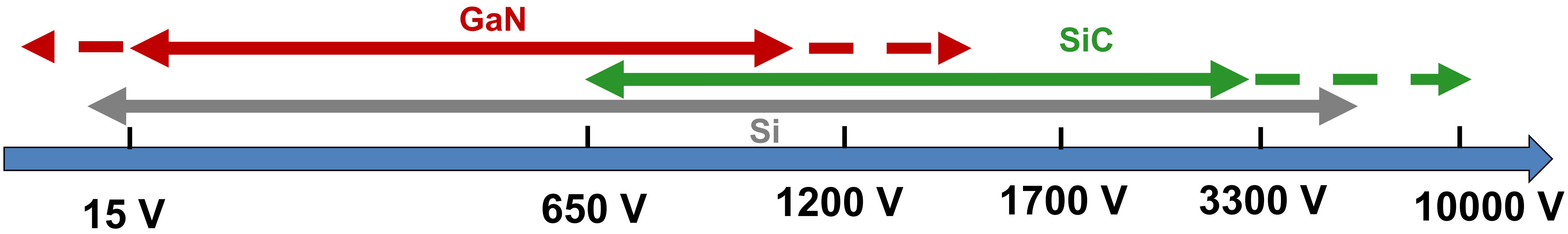
WBG Devices: GaN HEMTs and SiC MOSFETs (>$3 billion market)



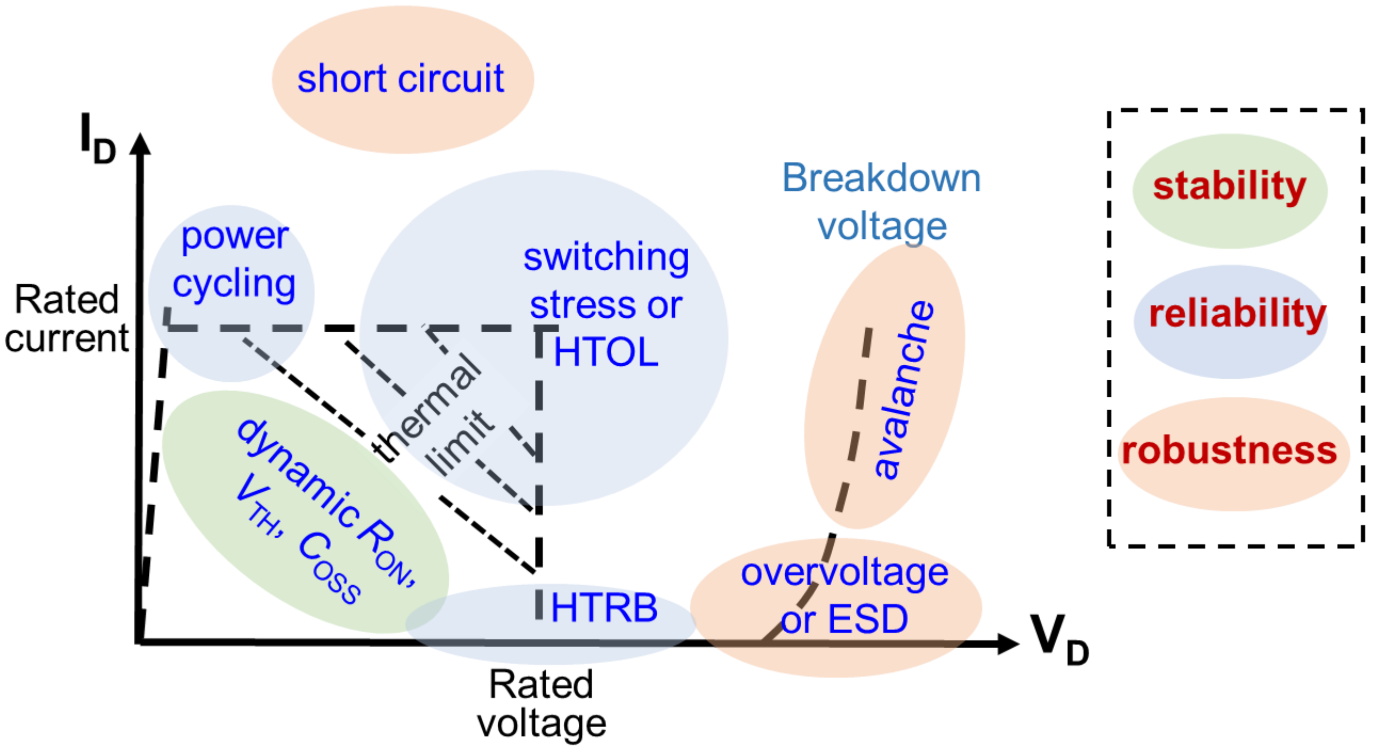
- √ 2DEG: mobility >1500 cm^2/Vs
- √ easy for IC integration
- × large chip size for high-voltage
- × thermal and E-field management
- × robustness (avalanche and short-circuit)



- × MOS: mobility ~100 cm^2/Vs
- × Mostly discrete
- √ high current
- √ small chip size for high-voltage
- √ easier thermal management



Stability, reliability, and robustness – framework



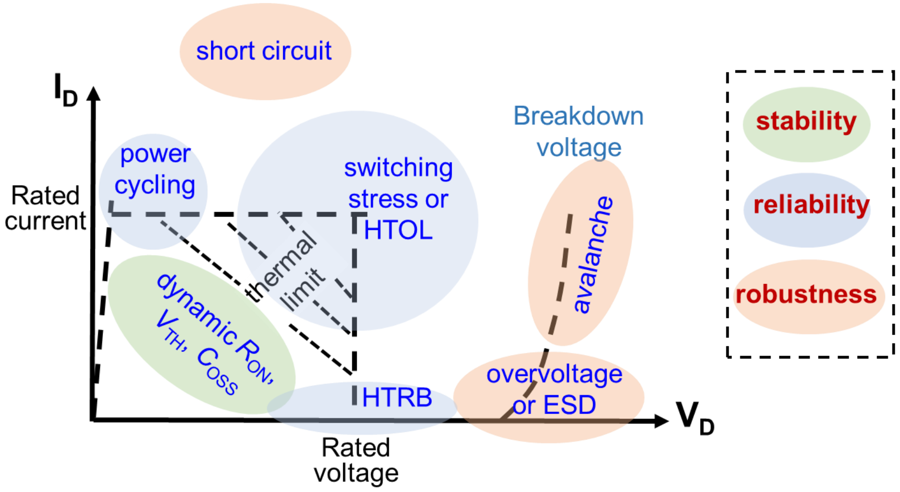
J. Kozak *et al.*, "Stability, reliability, and robustness of GaN power devices: a review," IEEE Trans. Power Electron., 2023

Why GaN is special?

- Dynamic stability
    - Dynamic R_{ON}: conduction loss
    - Hysteresis C_{OSS} loss: high-frequency switching loss
- Overvoltage and surge energy robustness
    - No avalanche capability
- Short circuit robustness
- Gate reliability and robustness
- Must be characterized under inductive switching conditions

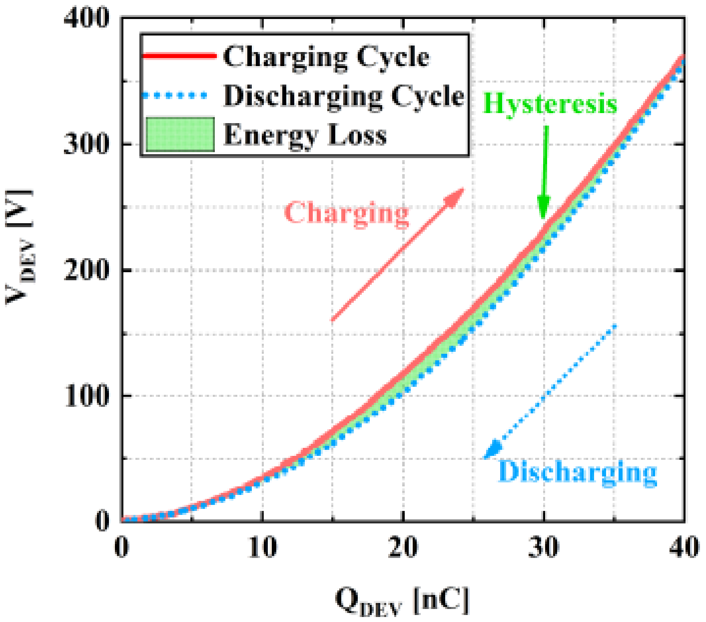
Outline

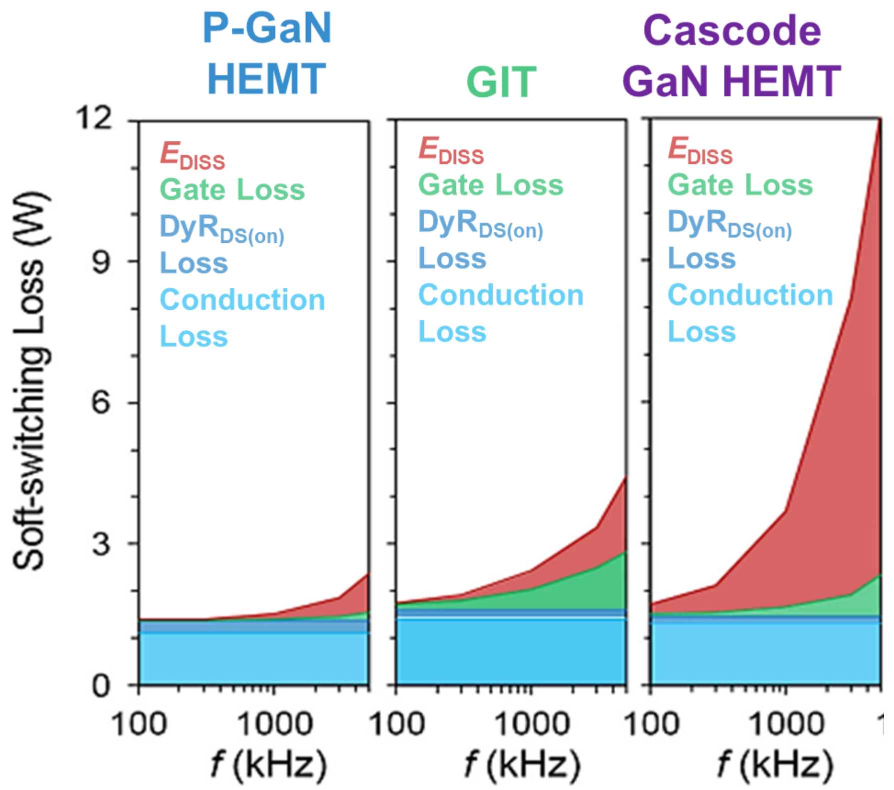
- **Lateral GaN HEMT Reliability**
  - Output capacitance loss
  - Overvoltage robustness and lifetime
  - Gate reliability and lifetime
- **Bidirectional GaN**
- **Vertical GaN Devices: Performance and Reliability**
  - Dynamic R_{ON}, avalanche, short-circuit
  - MHz converter application
- **Summary**



Hysteresis C_{OSS} loss

- ***C_{OSS}* loss: generated when *C_{OSS}* is charged and discharged in OFF-state (an ideal lossless process)**
- "Hysteresis Loss" : energy stored in C_{OSS} ≠ energy discharged from C_{OSS}



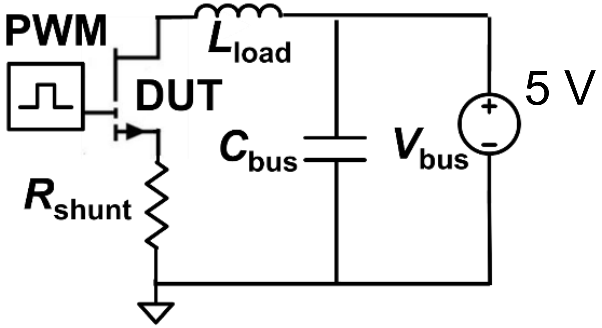


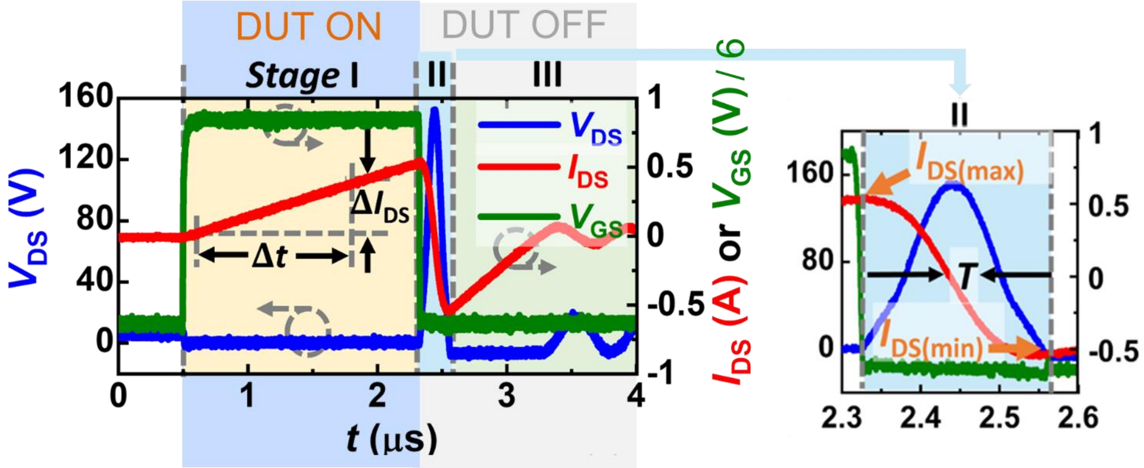
- A potential issue for GaN HEMTs, especially at (very) high-frequencies soft-switching applications, i.e., at MHz level.

G. Zulauf *et al*., IEEE Trans. on Power Electron., 2018.

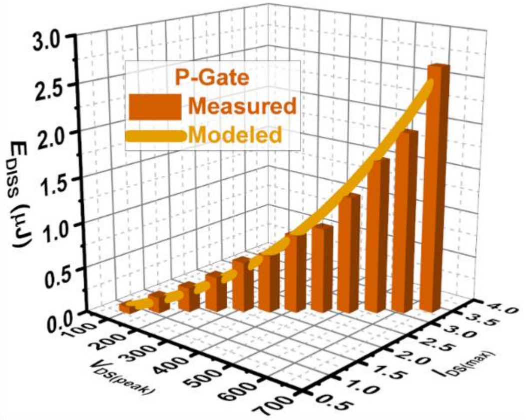
A. Jafari *et al*., IEEE Trans. on Power Electron., 2020.

C_{OSS} loss characterization and modeling – discrete GaN





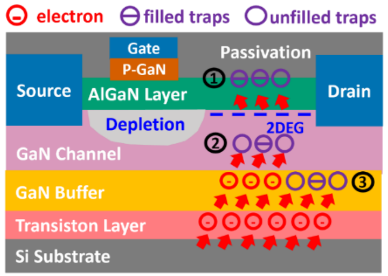
- L_{load} resonates with DUT's C_{OSS}
- Minimal turn-off loss
- C_{OSS} loss extracted from the resonance



$$P_{OSS} = f_{SW} k[\alpha + \beta I_{DS(max)}] V_{DS(peak)}^{\gamma}$$

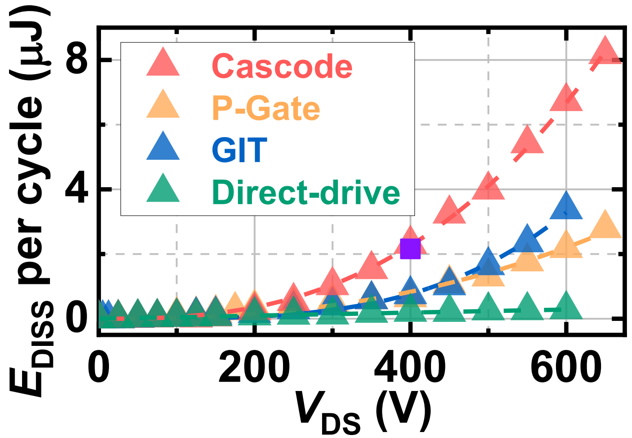
f_R	DUT	k	α	β	γ
2 MHz	P-gate	1.45×10^{-11}	0.42	0.33	1.86
	HD-GIT	0.95×10^{-16}	0.54	0.37	3.42
	Direct-drive	4.12×10^{-10}	0.03	0.30	1.20
6.78 MHz	P-Gate	1.81×10^{-11}	0.36	0.18	1.84
	HD-GIT	2.51×10^{-15}	0.29	0.22	3.32
	Direct-drive	2.58×10^{-11}	0.01	0.20	1.69

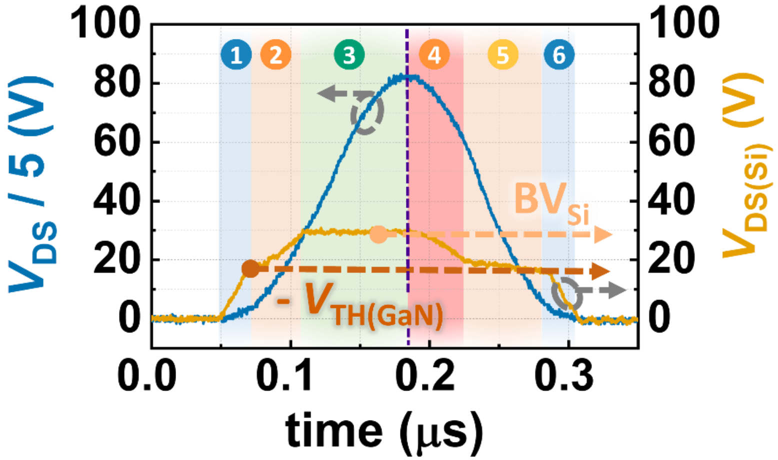
- E_{DISS} dependent on resonance frequency (dv/dt), voltage (power law), and current (linear), weak dependence on T
- Related to fast traps, with de-trapping time constants distinct from dynamic R_{on}

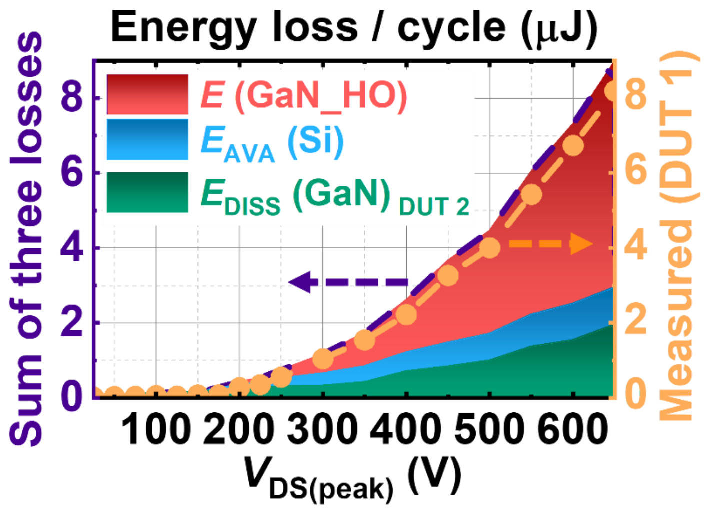


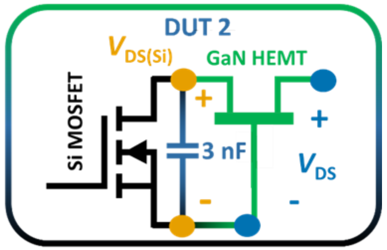
Q. Song *et al.*, "Output Capacitance Loss of GaN HEMTs in Steady-State Switching," IEEE Trans. on Power Electron., 2023.

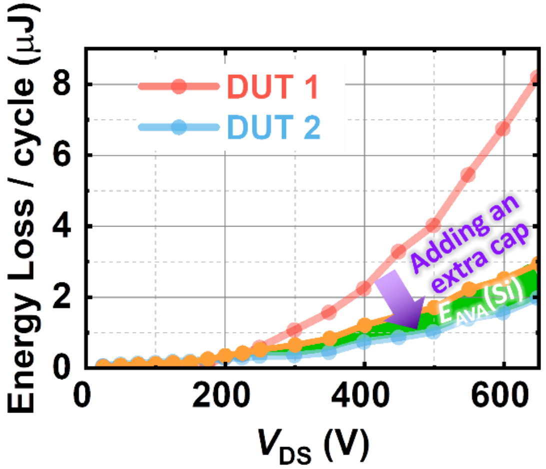
Higher C_{OSS} loss in GaN Cacode: two additional origins









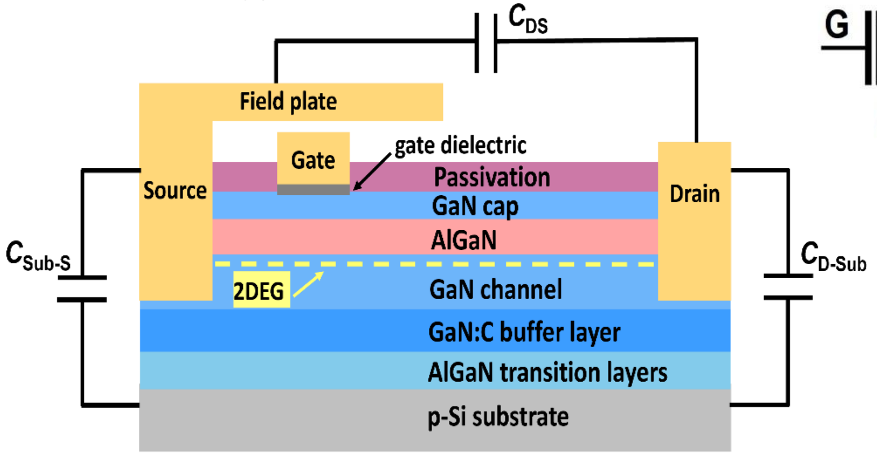


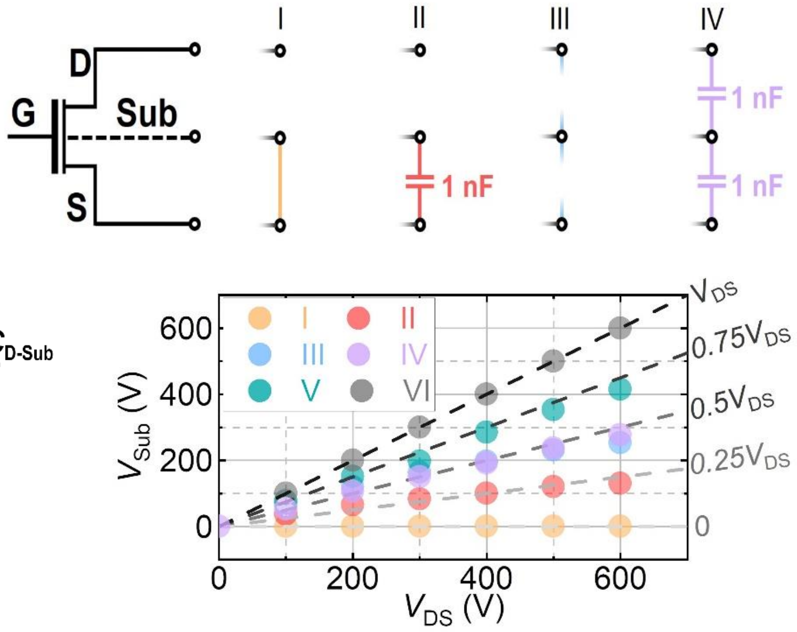
- C_{OSS} loss much higher in GaN cascode devices
- #1: C_{OSS} loss in GaN HEMT
- #2: Si avalanche loss
- #3: GaN hard turn-on loss (could be dominant)
- #2 and #3 are both due to Si avalanche in GaN cascode
- Solution: increasing Si C_{OSS} to make an avalanche-free cascode -> 75% less loss in soft switching

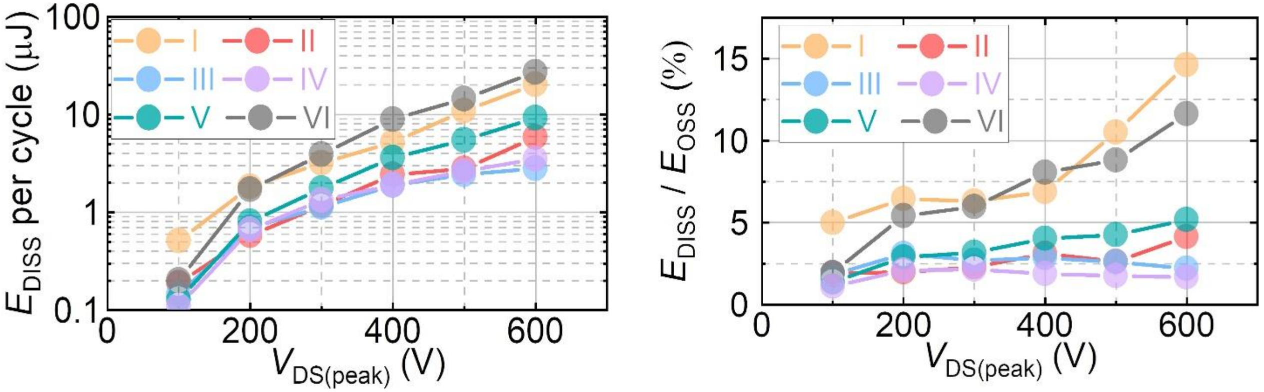
POWERAMERICA

Q. Song *et al.*, "Origin of Soft-Switching Output Capacitance Loss in Cascode GaN HEMTs at High Frequencies," IEEE Trans. on Power Electron., 2023.

Minimizing intrinsic C_{OSS} loss in GaN HEMT







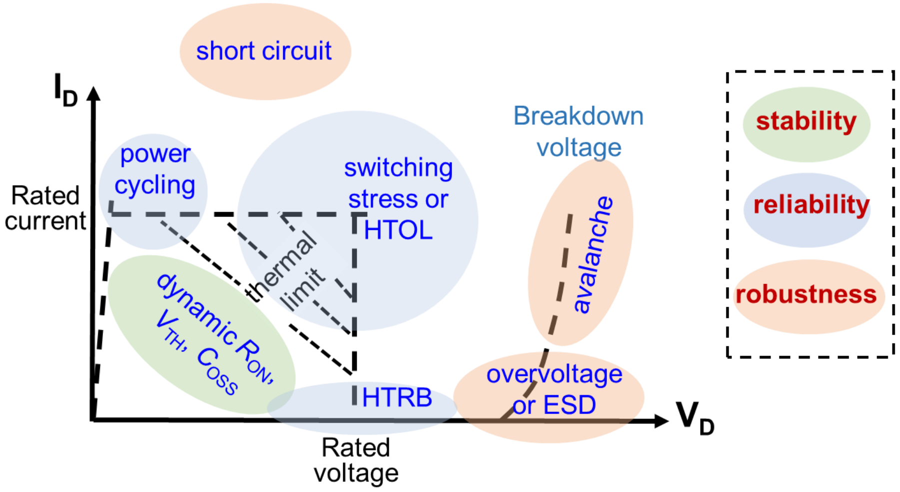
- C_{OSS} loss of GaN-on-Si HEMT can be reduced by tuning the substrate bias (V_{SUB}) in dynamic switching
- Compared to sub-source-shorting, at $V_{SUB} = 0.5V_{DS}$, E_{DISS} reduced by up to 86%, E_{DISS}/E_{OSS} ratio decreased from 14.6% to 2.2%
- Physics related to depletion front profile at different V_{SUB}

VisIC TECHNOLOGIES

Q. Song *et al.*, "Minimizing Output Capacitance Loss in GaN Power HEMT," IEEE Trans. on Power Electron., 2024.

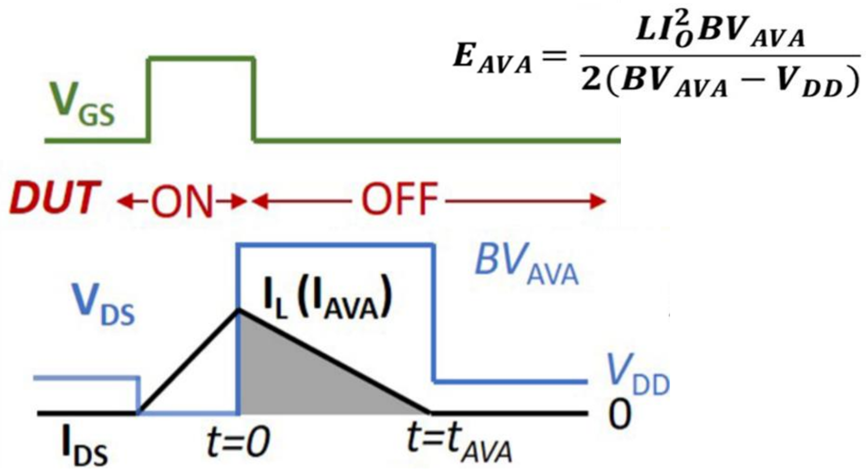
Outline

- **Lateral GaN HEMT Reliability**
  - Output capacitance loss
  - Overvoltage robustness and lifetime
  - Gate reliability and lifetime
- **Bidirectional GaN**
- **Vertical GaN Devices: Performance and Reliability**
  - Dynamic R_{ON}, avalanche, short-circuit
  - MHz converter application
- **Summary**

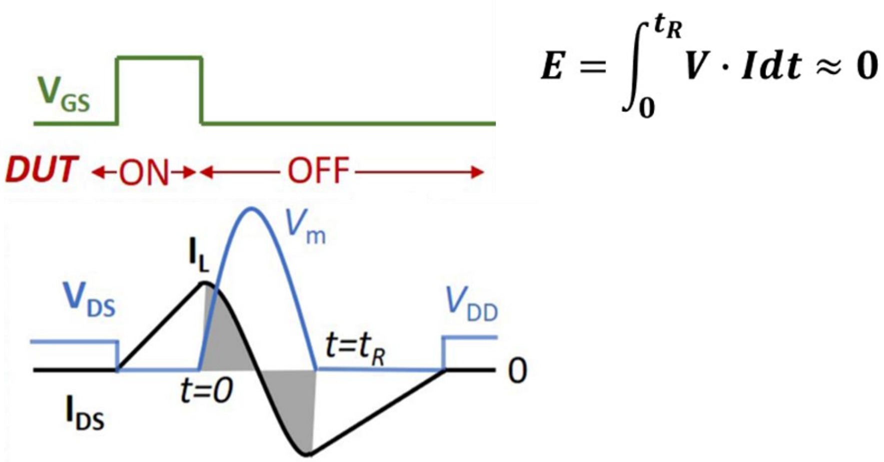


Surge-energy robustness: Si/SiC MOSFETs v.s. GaN HEMTs

Si & SiC MOSFET:



GaN HEMT:

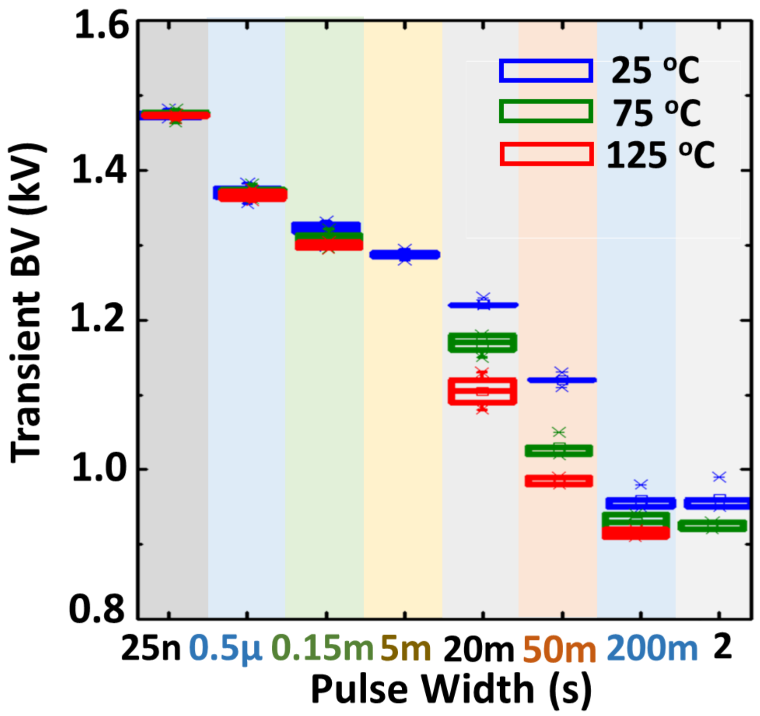


Withstand process	avalanching	LC resonance & reverse conduction
Energy path	dissipation in device in avalanching	little/no dissipation in withstand; dissipation in reverse conduction
Limiting factor	avalanche energy	overvoltage capability
Failure mechanism	thermal run-away	E-field induced breakdown

R. Zhang *et al*., “Surge energy and overvoltage ruggedness of p-gate GaN HEMTs”, IEEE Trans. Power Electron., 2020

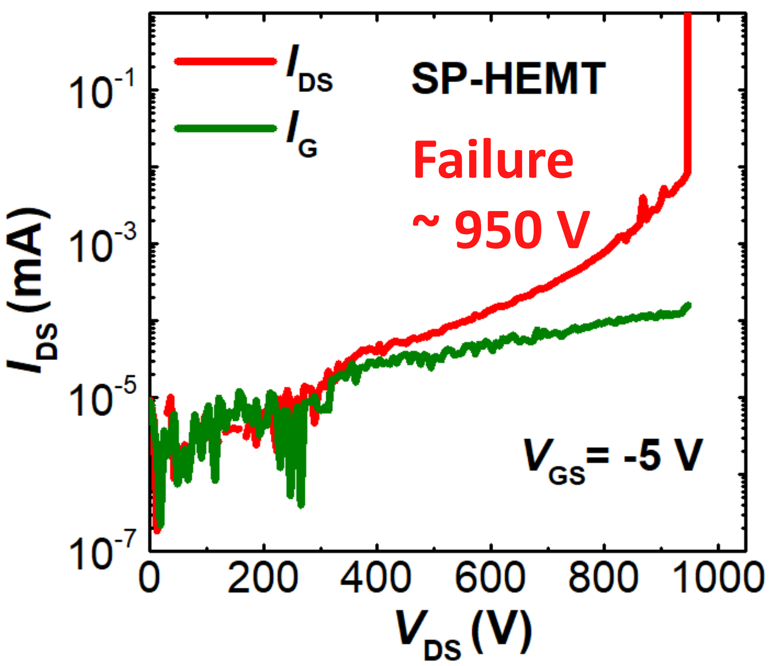
Dynamic breakdown voltage

Inductive Switching Circuit



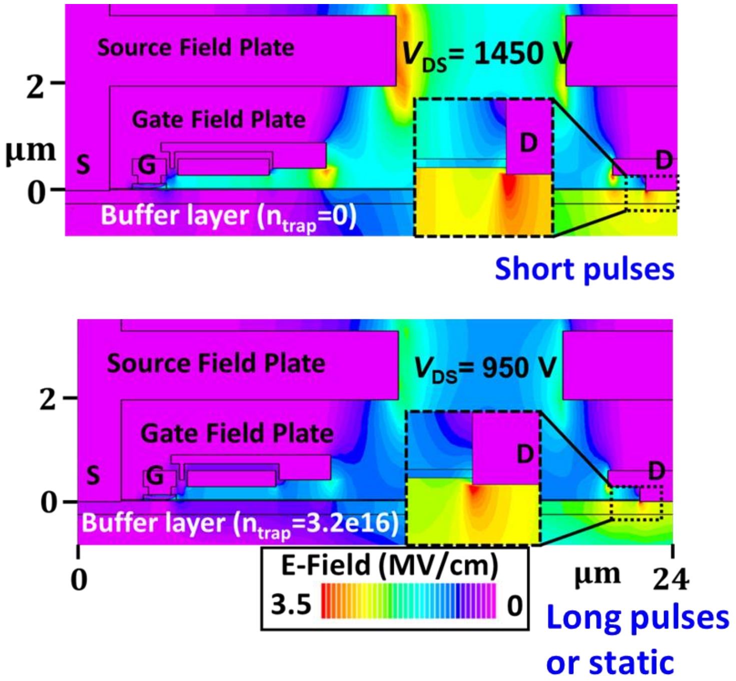
- BV reduce with pulse width

Quasi-static I-V sweep



- BV converges to 'static' BV when PW> 200 ms
- Dynamic BV > Static BV

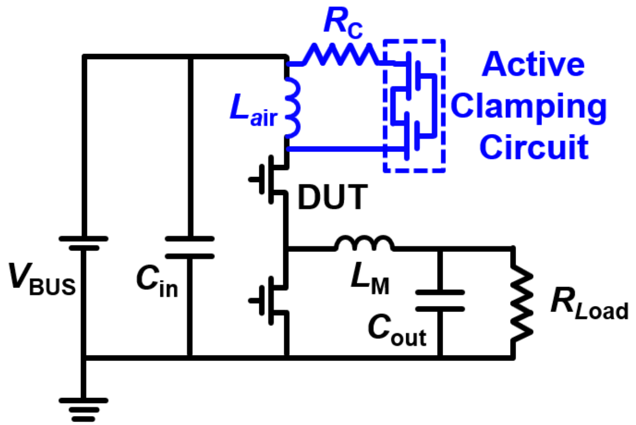
Physical mechanism

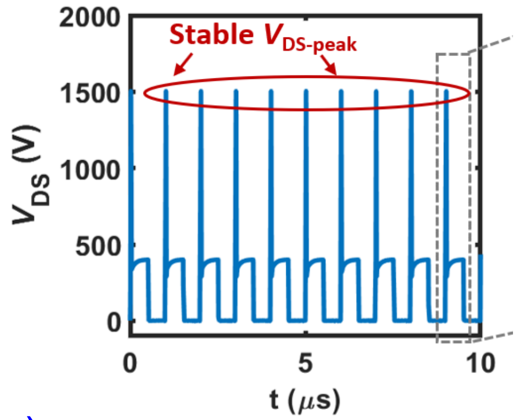


- Time-dependent buffer trapping
- Impact peak E-field

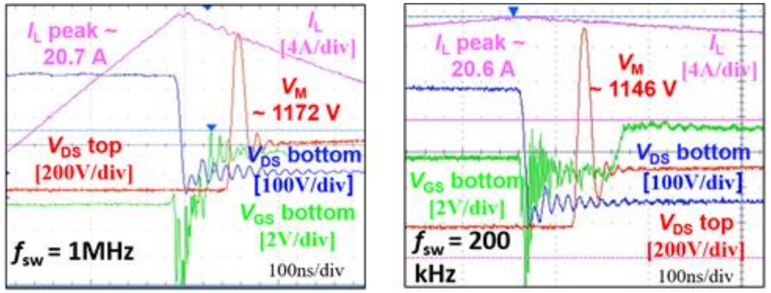
R. Zhang *et al*., "Dynamic breakdown voltage of GaN power HEMTs", IEDM, 23.3, 2020

Overvoltage switching at high frequency up to Megahertz





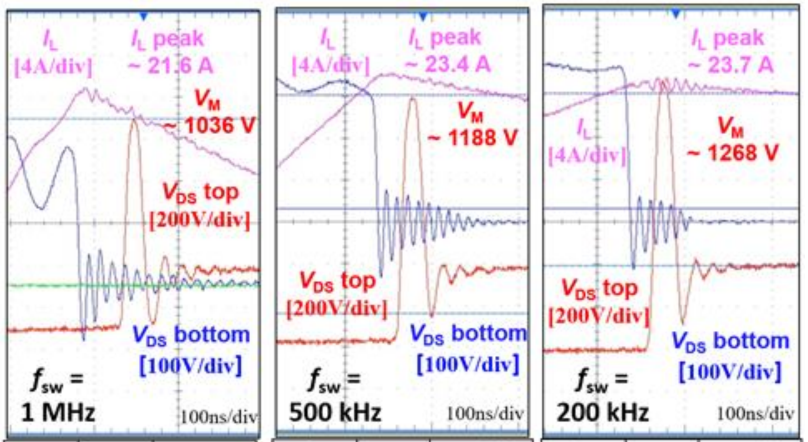
HD-GIT



f_{sw}	#	V_M (V)
1 MHz	1	1172
	2	1156
	3	1127

f_{sw}	#	V_M (V)
200 kHz	1	1146
	2	1171
	3	1163

SP-HEMT (BV drop at higher f_{sw})

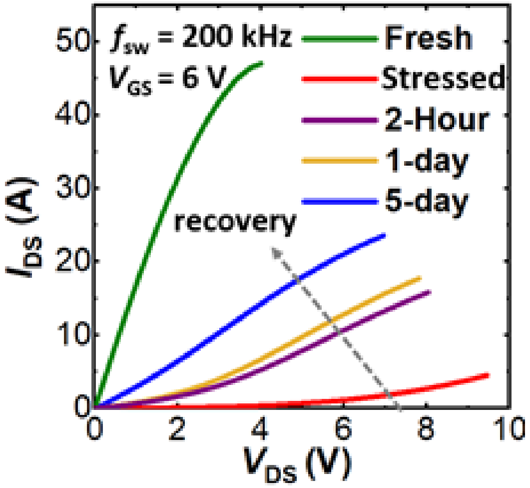


f_{sw}	#	V_M (V)
1 MHz	1	1036
	2	1060
	3	1040

f_{sw}	#	V_M (V)
500 kHz	1	1188
	2	1188
	3	1192

f_{sw}	#	V_M (V)
200 kHz	1	1268
	2	1264
	3	1268

Repetitive UIS @ 75% BV



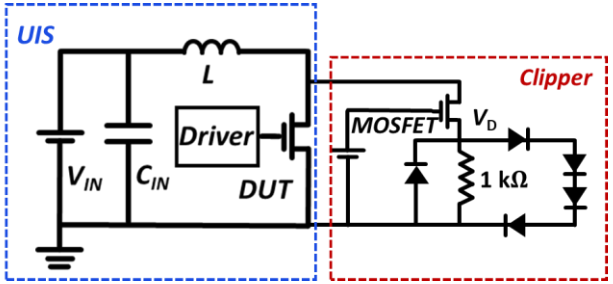
- Overvoltage switching at high f_{SW} triggers a new failure mechanism: thermal failure due to significant dynamic R_{ON} increase
- Qualification method: repetitive UIS
- Dynamic R_{ON}: the true limiter for overvoltage lifetime?

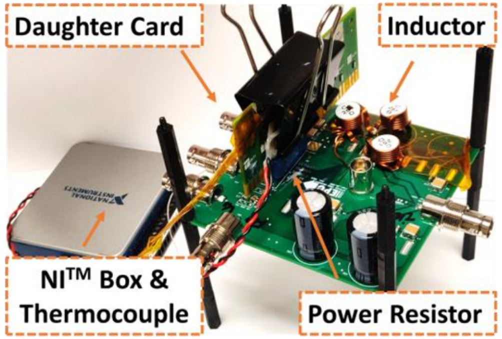
R. Zhang et al., "Overvoltage Robustness of p-Gate GaN HEMTs in High Frequency Switching up to Megahertz", IEEE Trans. Power Electron., 2023

Device lifetime under overvoltage switching: limited by dynamic R_{on}

Voltage rating can be determined by long-term dynamic R_{ON} increase (e.g., 10% after 10-yr hard-switching)

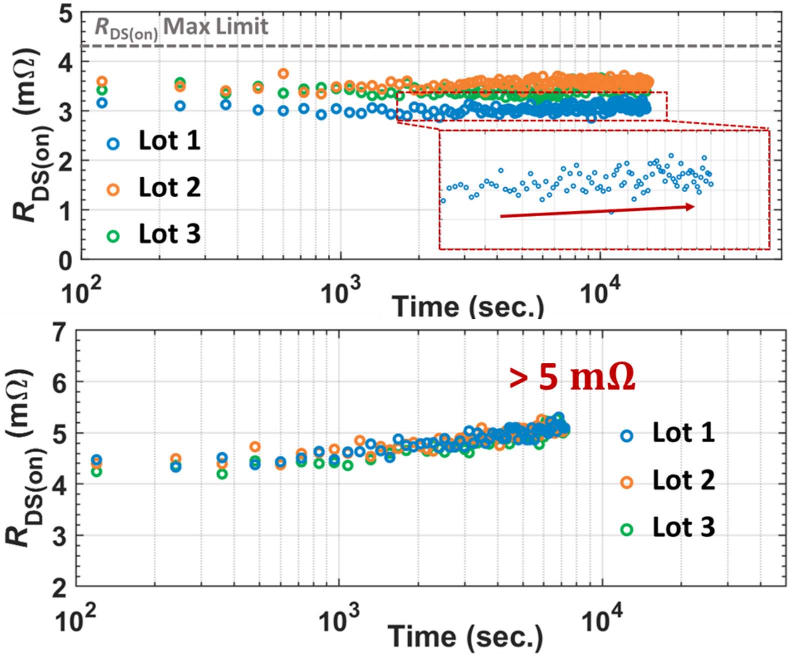
In-situ monitoring of R_{ON}



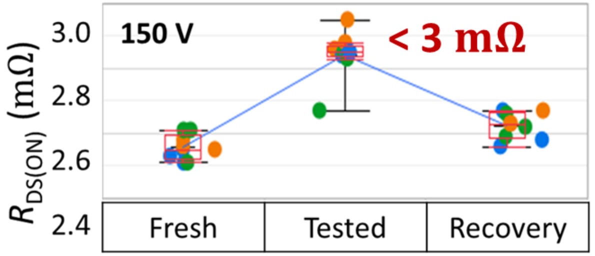


Dynamic R_{ON} increase is the major degradation in overvoltage switching

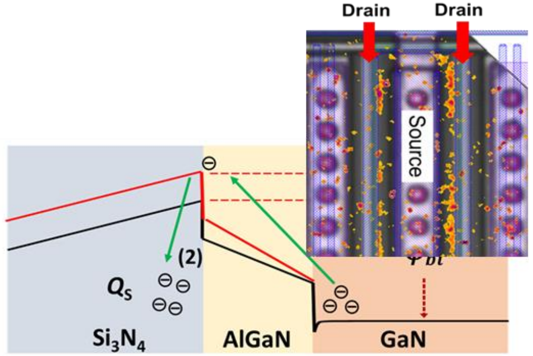
DUT: EPC2218 (100 V rated) f_{sw} : 100 kHz
V_{DS} peak : 120 & 150 V T_C : 75 °C



Cannot be captured by off-line measurement



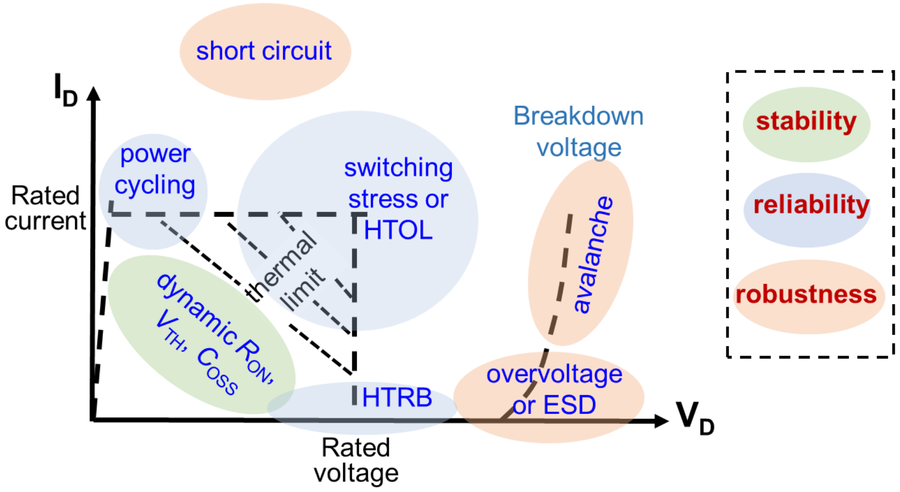
Physics-based model for lifetime projection



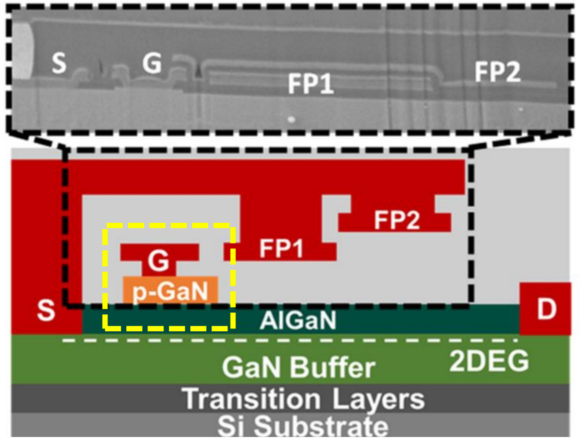
R. Zhang *et al*., "In-situ RDS(on) Characterization and Lifetime Projection of GaN HEMTs Under Repetitive Overvoltage Switching," IEEE Trans. Power Electron., 2023

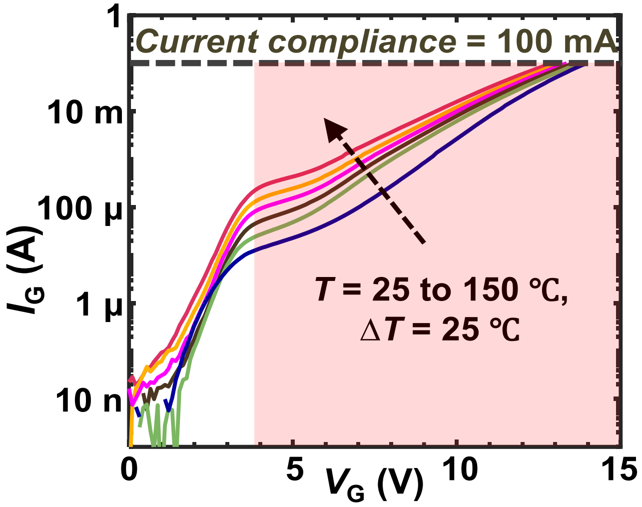
Outline

- **Lateral GaN HEMT Reliability**
  - Output capacitance loss
  - Overvoltage robustness and lifetime
  - Gate reliability and lifetime
- **Bidirectional GaN**
- **Vertical GaN Devices: Performance and Reliability**
  - Dynamic R_{ON}, avalanche, short-circuit
  - MHz converter application
- **Summary**

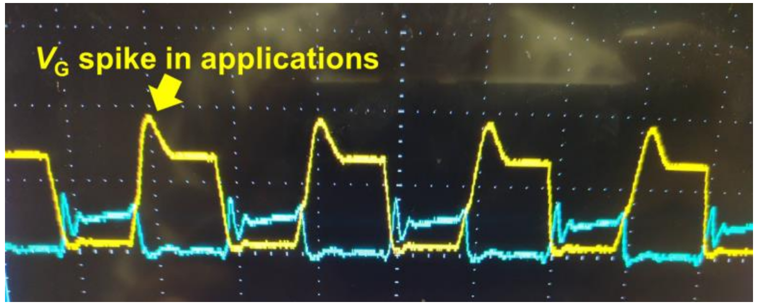


Small V_{GS} headroom of p-gate GaN HEMT (as low as 1V)

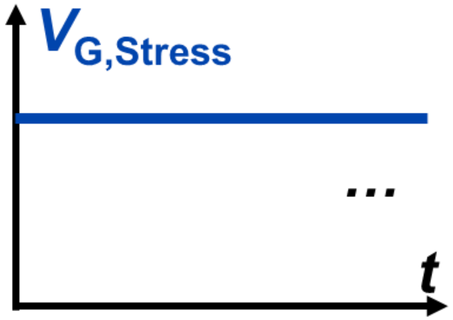




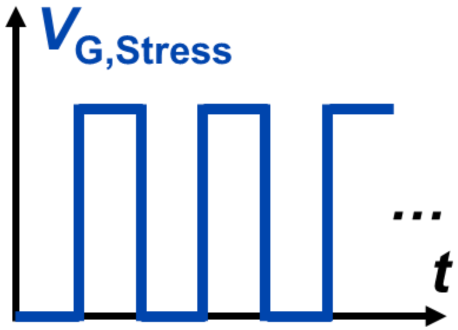
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient For ≤ 1 μs	$V_{GS(transient)}$	-20 to +10	V



Prior methods



DC stress

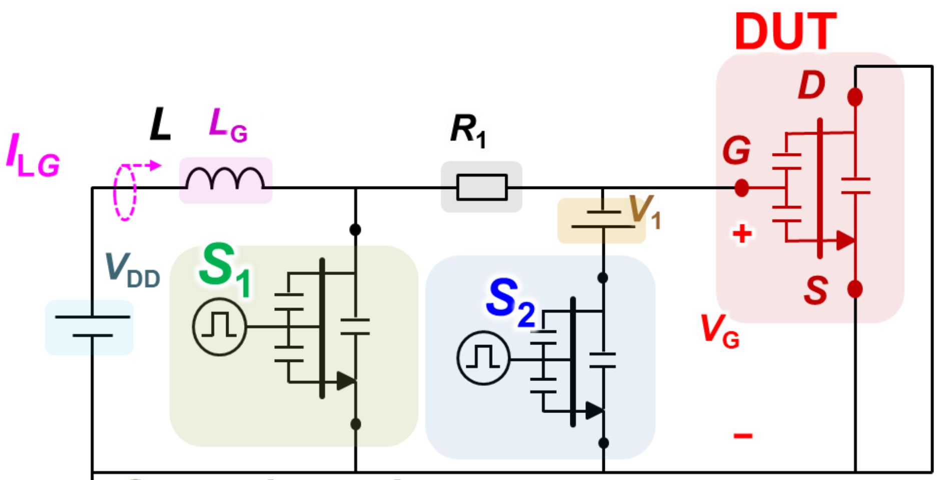


Pulse-IV (AC square)

- **Not RLC-resonant-like**
- **Slow turn on (low dV_G/dt)**
- **No power loop switching (i.e., drain-source grounded)**

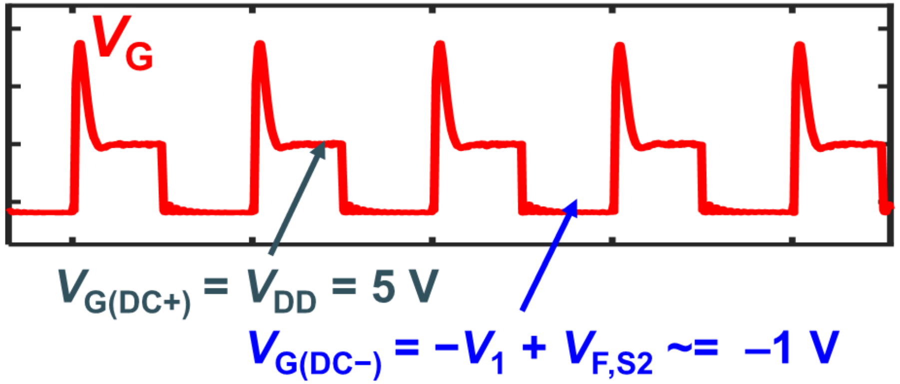
B. Wang et al. "Gate Robustness and Reliability of P-Gate GaN HEMT Evaluated by a Circuit Method.“ IEEE Trans. Power Electron., 2024

Gate reliability evaluated by circuit method

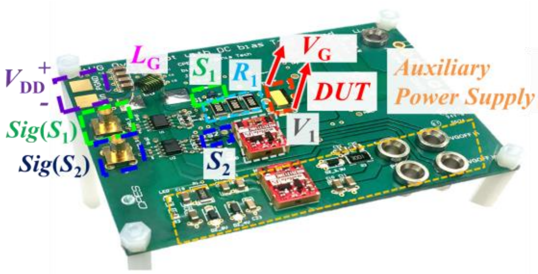


S_1 ON: charge L_G for surge energy

S_2 ON: pull down V_G (< 0), mimic OFF-state



Spec.	Symbol	Functionality	Typ. Value
Input DC V.	V_{DD}	• $V_{G(DC+)} = V_{DD}$ • Charge L_G	5 V
Gate-loop inductor	L_G	• Store surge energy • Modulate overshoot pulse width	50nH ~ 120nH
Fast switch	S_1	• When ON, L_G charged by V_{DD}	EPC8010
S_1 ON-time	$t_{ON,S1}$	• Modulate $V_{G(PK)}$ via surge energy	20ns ~ 100ns
Iso. DC V.	V_1	• $V_{G(DC-)} \sim -V_1$	1 V
Fast switch	S_2	• When ON, pull down V_G (< 0)	EPC8002
S_2 ON-time	$t_{ON,S2}$	• Modulate D (via OFF time)	50ns ~ 50μs
Power resistor	R_1	• Dissipate power of DC V. • Damp ringing	33 Ω



B. Wang *et al*. "Gate Switching Lifetime of P-Gate GaN HEMT: Circuit Characterization and Generalized Model." IEEE Trans. Power Electron., 2024

Gate switching lifetime model (arbitrary V_G waveform, T, f_{sw})

- **Voltage Acceleration Function:**

$$\sum stress^V = \int_0^T [V_G(t) - V_{G,Th}]^b dt \times \#SCTF$$

- **f_{sw} Acceleration Function:**

$$AF^{f_{SW}} = \begin{cases} 1 & (f_{SW} \le f_{Th}) \\ d \cdot f_{SW}{}^{e} & (f_{Th} < f_{SW} < f_{Sat}) \\ d \cdot f_{Sat}{}^{e} & (f_{SW} > f_{Sat}) \end{cases}$$

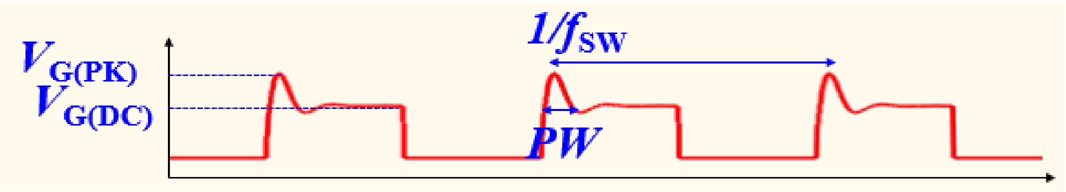
$(e = 0.6)$

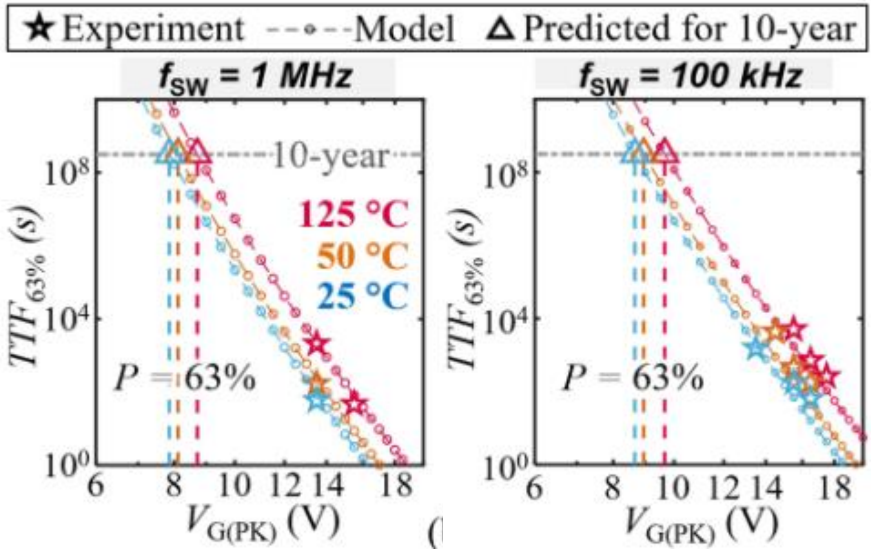
- ***T* Acceleration Function:**

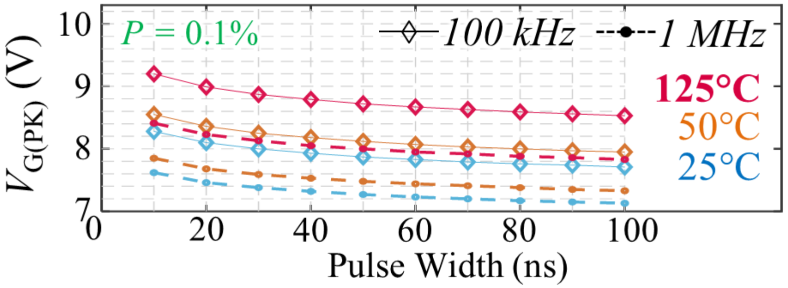
$$AF^T = \exp\left(-\frac{E_A}{kT}\right) \quad (E_A \sim -0.3\text{ eV})$$

- ***Full switching model*:**

$$TTF = \frac{\#SCTF}{f_{SW}} = \frac{Const.}{\int_0^T [V_G(t) - V_{G,Th}]^{26} dt \times f_{SW} \times AF^{f_{SW}} \times exp\left(\frac{0.3eV}{kT}\right)}$$

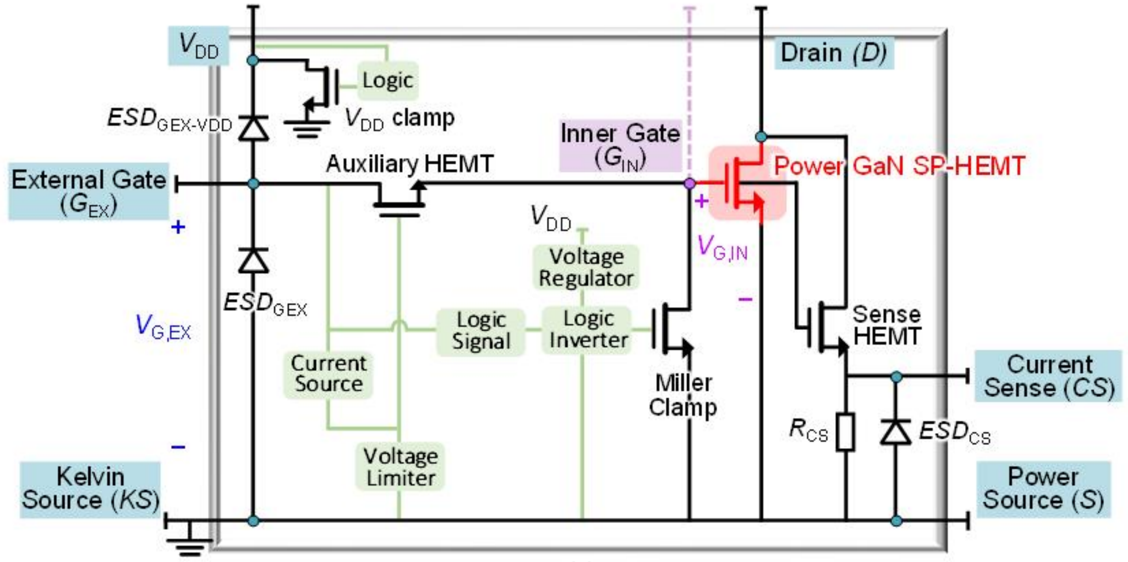


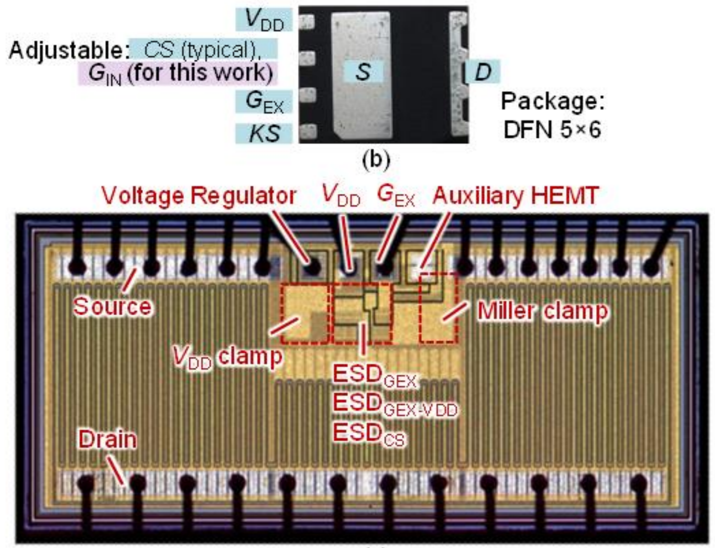


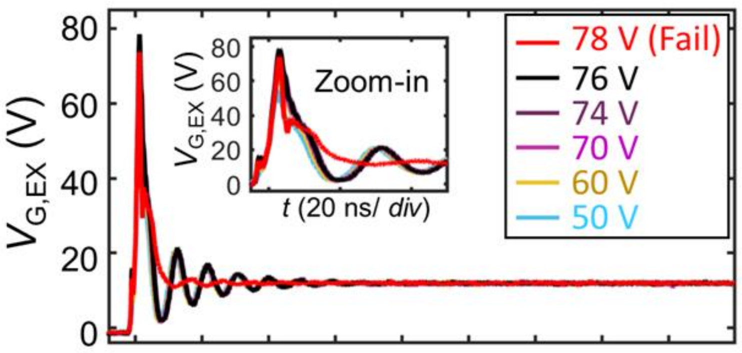


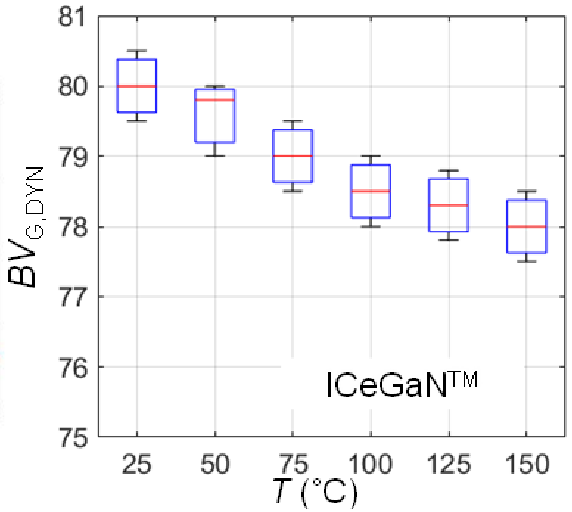
B. Wang *et al*. "Gate Switching Lifetime of P-Gate GaN HEMT: Circuit Characterization and Generalized Model." IEEE Trans. Power Electron., 2024

Gate robustness improvement by monolithic IC









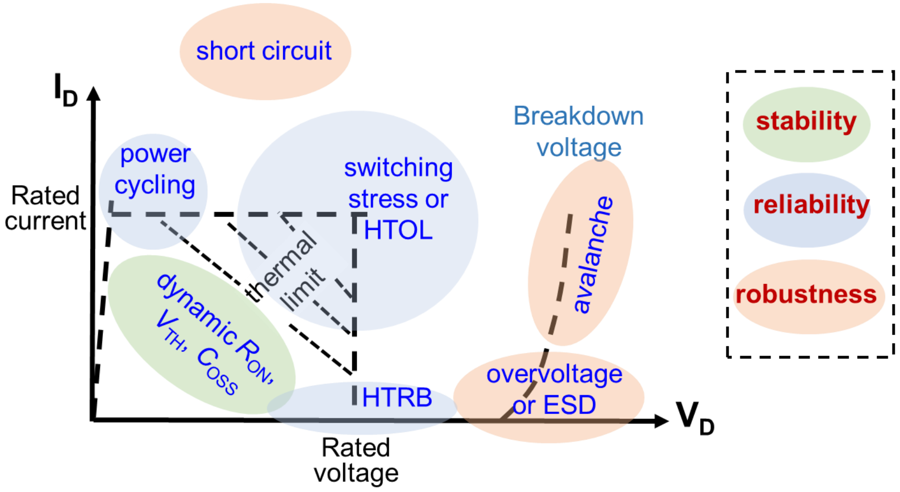
DUT	25 °C	150 °C
ICeGaN™	80 V	78 V
Si IGBT	80 V	80 V
SiC MOSFET	70 V	70 V
Discrete GaN SP-HEMT	24 V	25 V

- ICeGaN: GaN HEMT + monolithic gate protection IC
- Gate drive voltage similar to Si IGBT and SiC MOSFET
- Fast IC response in nanosecond voltage overshoot in the gate driver loop
- Dynamic gate breakdown voltage reaches 80 V
- Rated gate voltage for continuous switching over 30 V

B. Wang *et al*. "Exceptional Gate Overvoltage Robustness in P-Gate GaN HEMT with Integrated Circuit Interface", APEC 2024

Outline

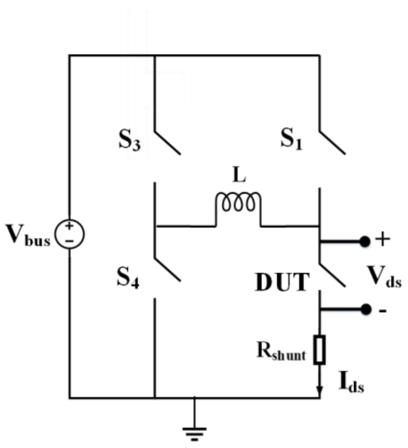
- **Lateral GaN HEMT Reliability**
  - Output capacitance loss
  - Overvoltage robustness and lifetime
  - Gate reliability and lifetime
- **Bidirectional GaN**
- **Vertical GaN Devices: Performance and Reliability**
  - Dynamic R_{ON}, avalanche, short-circuit
  - MHz converter application
- Summary



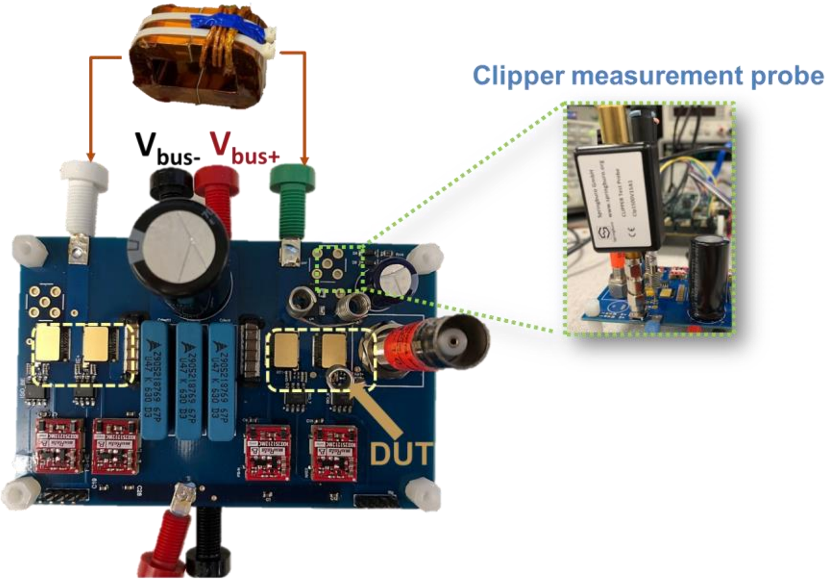
GaN Bidirectional Switch

Dynamic R_{ON} Evaluation Board for GaN BDS

- Evaluation of industrial bidirectional GaN HEMT with and without substrate bias management
- In-situ dynamic R_{on} and V_{th} evaluation circuits for bidirectional device in hard- and soft-switching



DPT measurement circuit

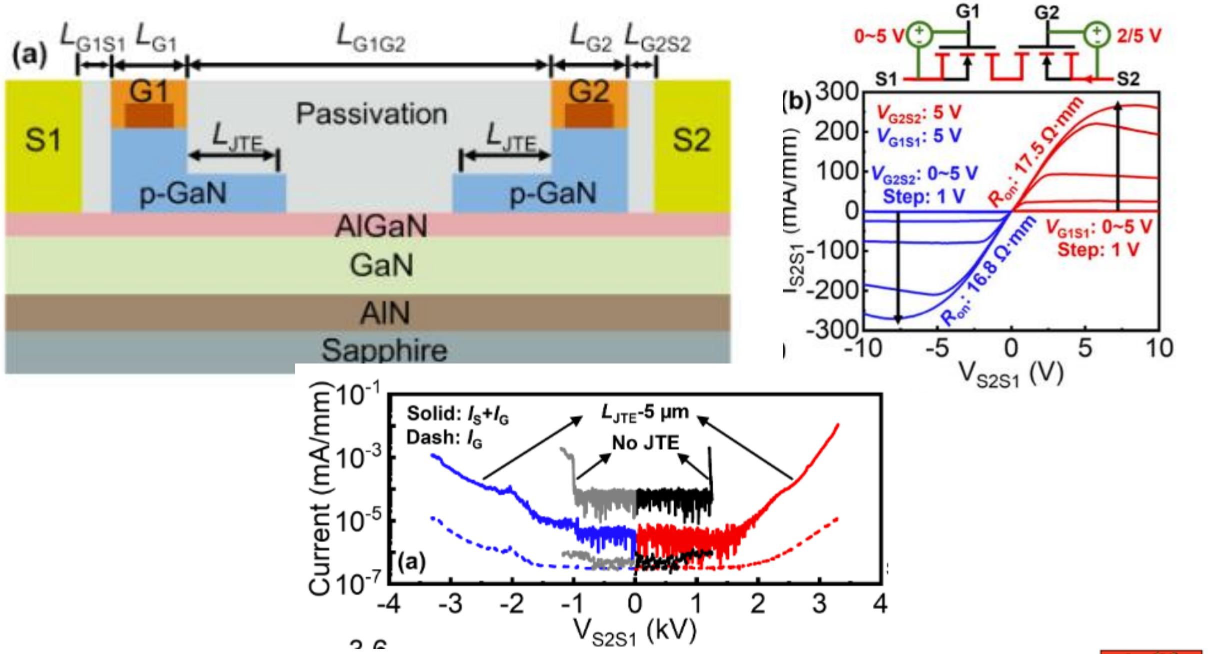


DPT measurement PCB board

Q. Song *et al*., APEC 2025, best presentation award

GaN BDS with Breakdown Votlage > 3 kV

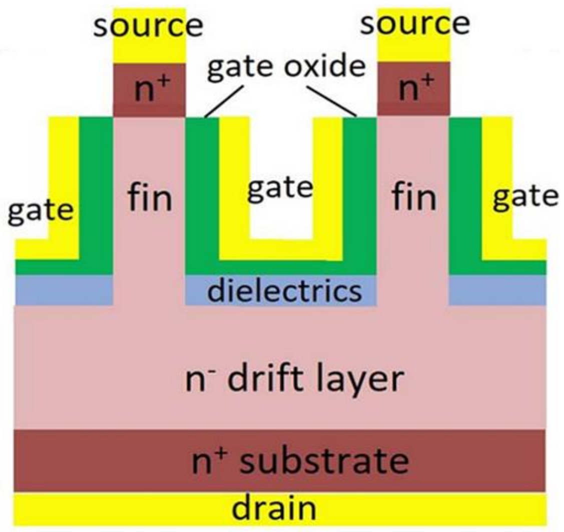
- GaN BDS with BV over 3.3 kV in both polarities
- Dual p-GaN JTE, E-mode, $R_{on,sp}$ of 5.6 mΩ·cm^2
- The highest BV and best FOMs in GaN and SiC MBDS

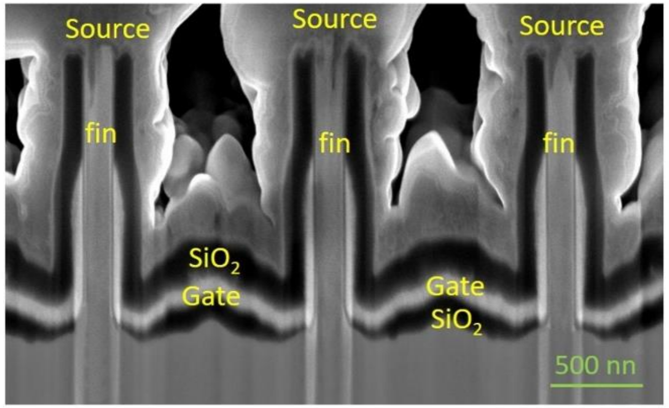


Y. Guo *et al*., "Enhancement-Mode GaN Monolithic Bidirectional Switch With Breakdown Voltage Over 3.3 kV," EDL 2025

Vertical GaN FinFET: from concept to commercialization

- 1.2 kV Fin-MOSFET with 200nm-wide fins
- V_{th}~1 V; $R_{on,sp}$= 1 mΩ·cm^2
- 2-inch GaN-on-GaN wafer process
- Superior $R_{ON}(Q_{OSS}+Q_{rr})$ than SiC

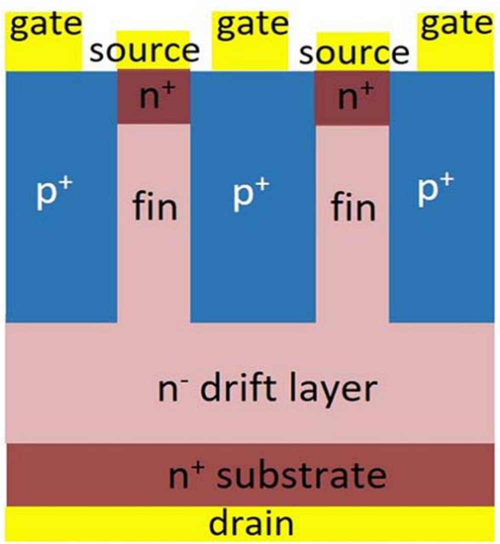


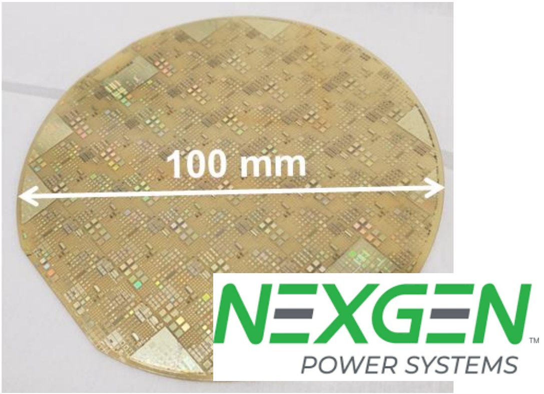


Y. Zhang *et al.*, **IEDM** 2017

Y. Zhang *et al.*, 40 (1), **EDL**, 2019
(2019 IEEE EDS George Smith Award)

- NexGen's 1.2 kV Fin-JFET commercialization (VT characterization & application)
- \$100M+ GaN-on-GaN Fab in Syracuse, NY
- 1470 V BV_{AVA}, avalanche capability, 0.82 mΩ·cm^2 (4-5x lower than 1.2 kV SiC MOS)

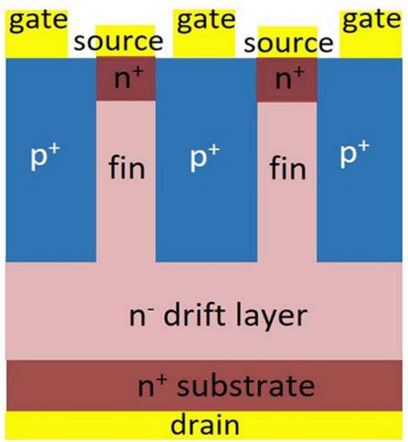


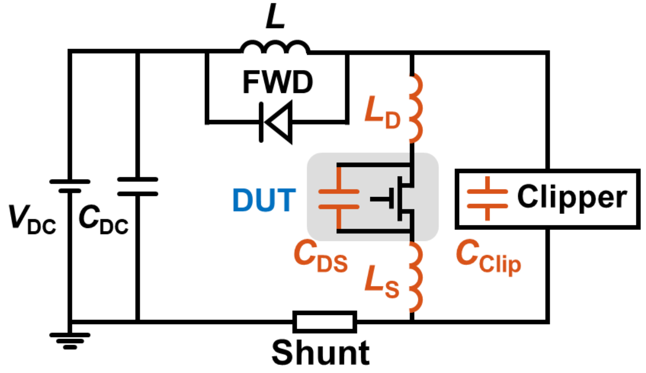


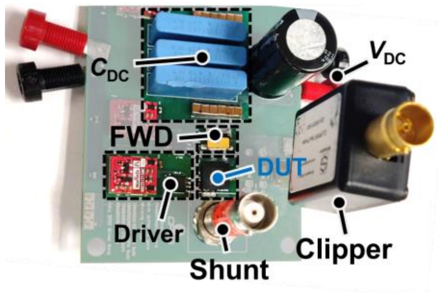
J. Liu *et al.*, **IEDM**, 23.2, 2020;
T-ED, 68, 2025, 2021

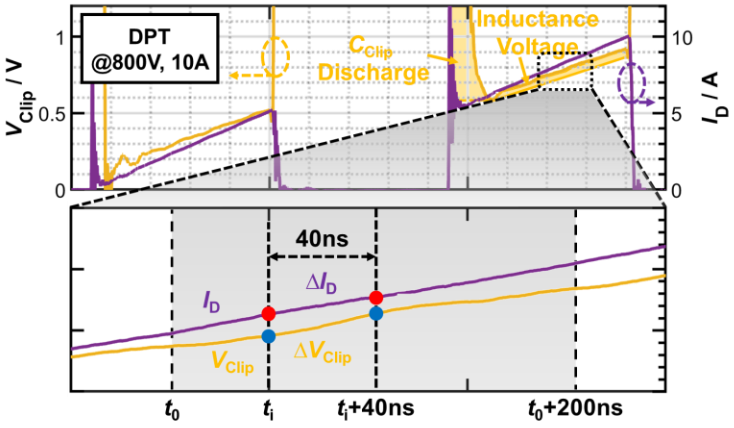
GaN devices can be dynamic R_{on} free

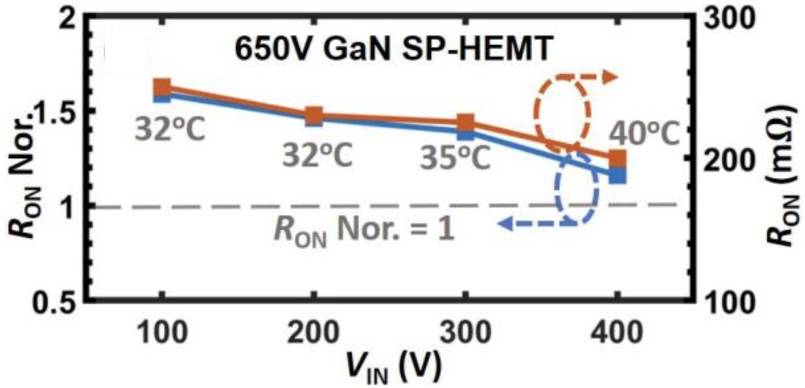
- Vertical GaN JFET are dynamic R_{ON} free under various voltage, current, temperature conditions
- Physics: 1) low dislocation density of GaN-on-GaN; 2) the absence of electric field crowding near the surface; 3) the minimal charge trapping in the native junction gate.

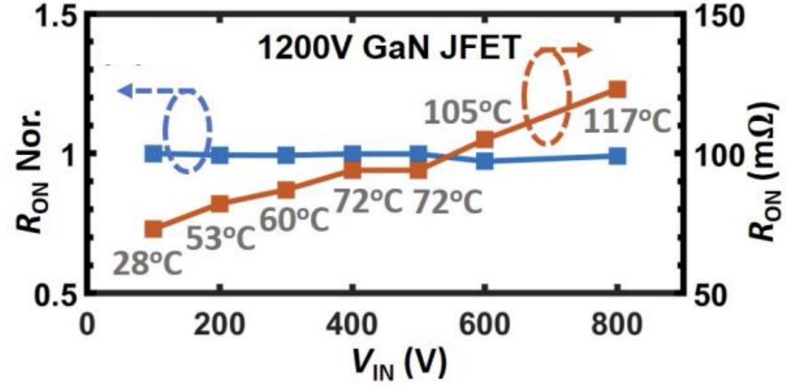










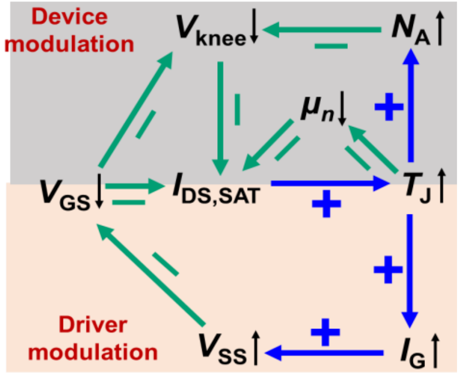


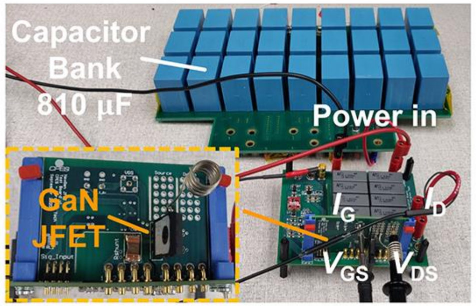
NEXGEN POWER SYSTEMS

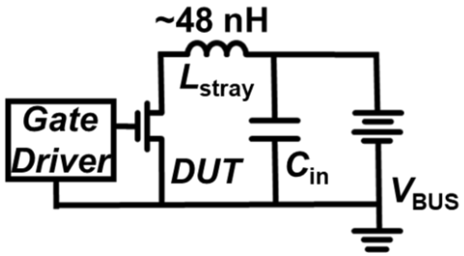
X. Yang *et al*., "Dynamic R_{ON} Free 1.2 kV Vertical GaN JFET," IEEE Trans. Electron. Dev., 2023

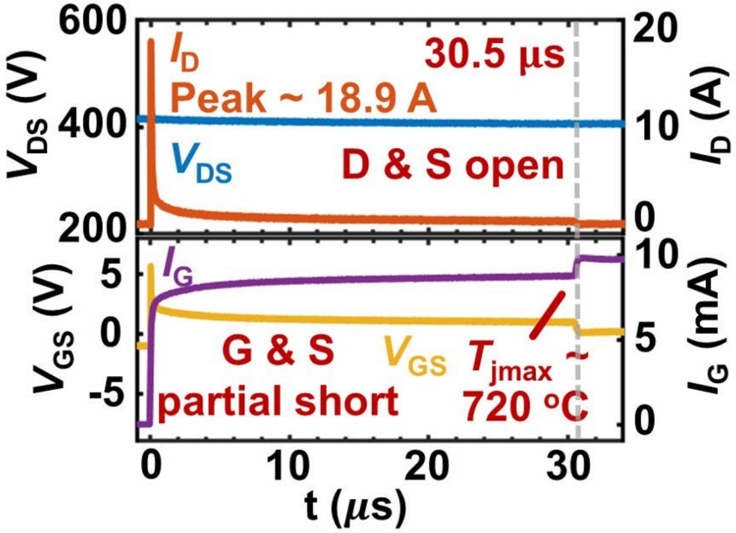
GaN devices can achieve breakthrough short-circuit robustness

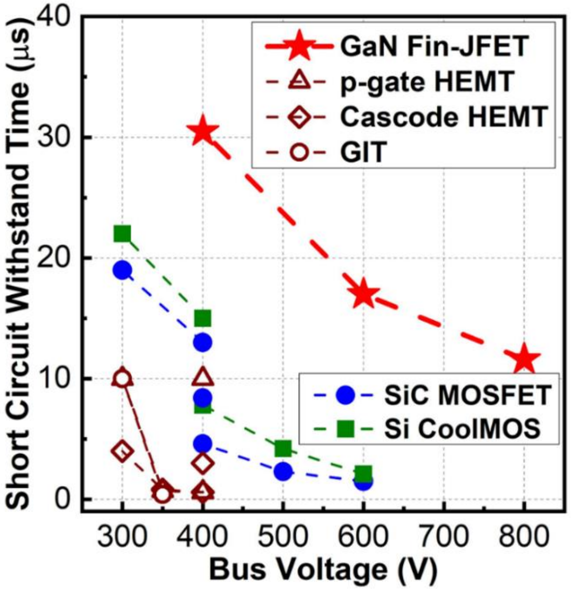
- 650V GaN JFET: 30.5 μs @ 400 V, 10.6 μs @ 800 V (BV_{AVA})
- 1200V GaN JFET: >40 μs @ 800 V
- Physics: device-driver circuit interplay to suppress I_{SAT} at high temp





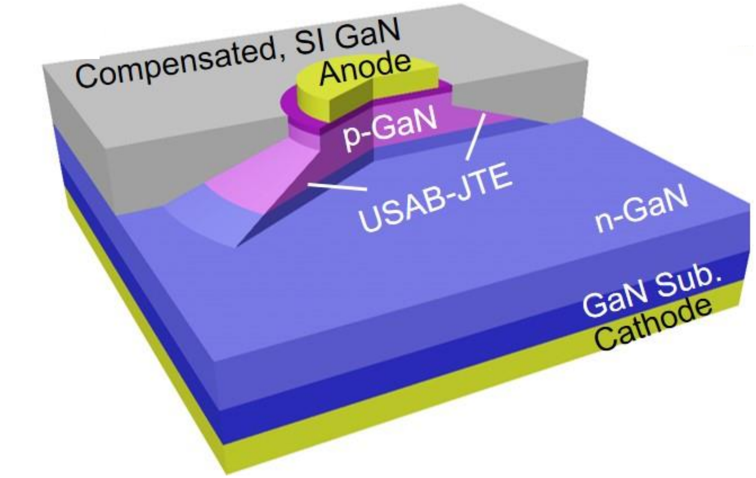


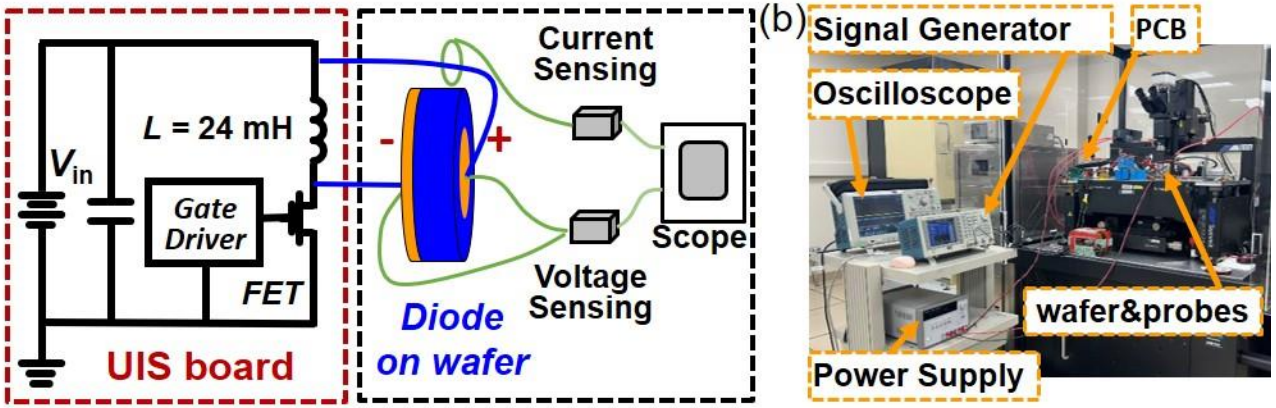


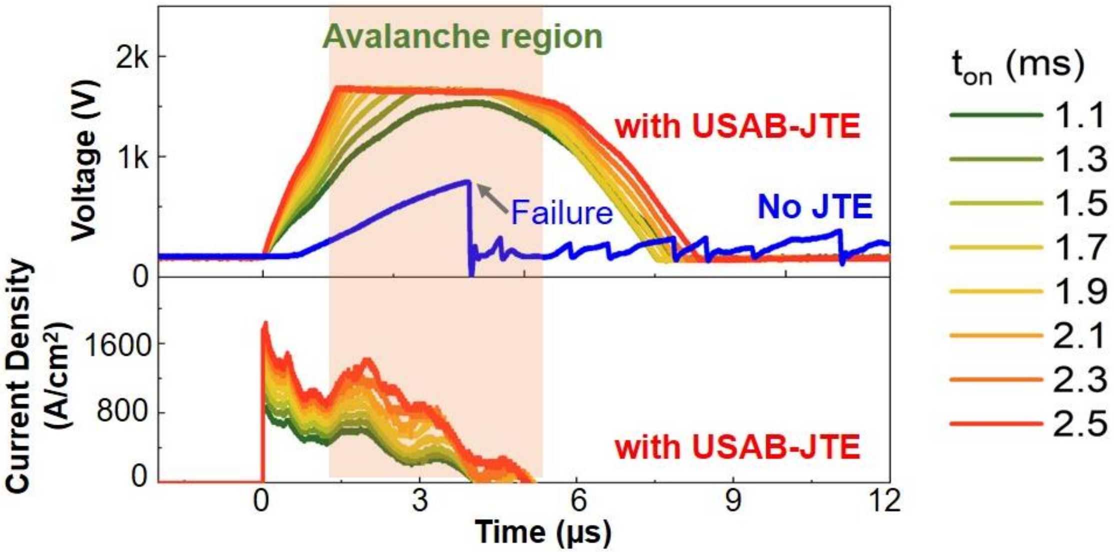


R. Zhang *et al.*, "Breakthrough short circuit robustness demonstrated in vertical GaN fin JFET," IEEE Trans. Power Electron. 2022
X. Yang *et al.*, "Evaluation and MHz Converter Application of 1.2-kV Vertical GaN JFET," IEEE Trans. Power Electron. 2024

GaN devices can have strong avalanche with right edge termination







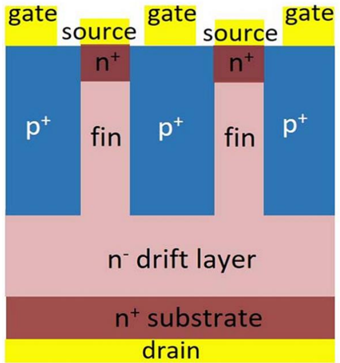
- True avalanche (high I_{AVA} @ BV_{AVA}) needs to be validated by avalanche circuit test
- Small-angle beveled JTE
- Fabricated by a single implantation into p-GaN using beveled PR or dielectric mask

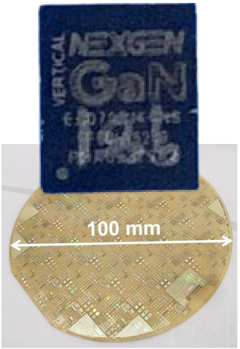
晶湛半导体 Enkris Semiconductor Nanowin

M. Xiao *et al*., "Robust avalanche in 1.7 kV vertical GaN diodes with a single-implant bevel edge termination," EDL, (**IEEE George Smith Award 2023**)

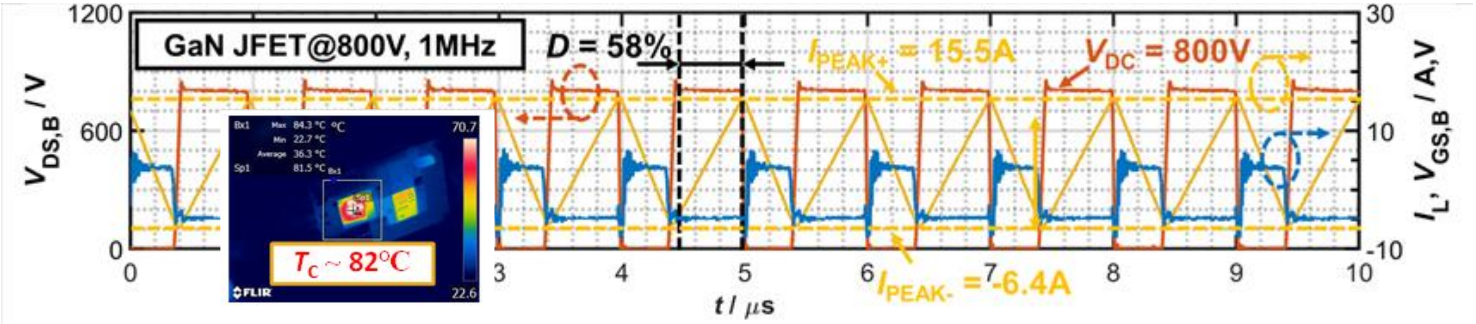
GaN power FinFET enables kilovolt, MHz applications

1.2kV,70mΩ GaN FinFET in DFN package

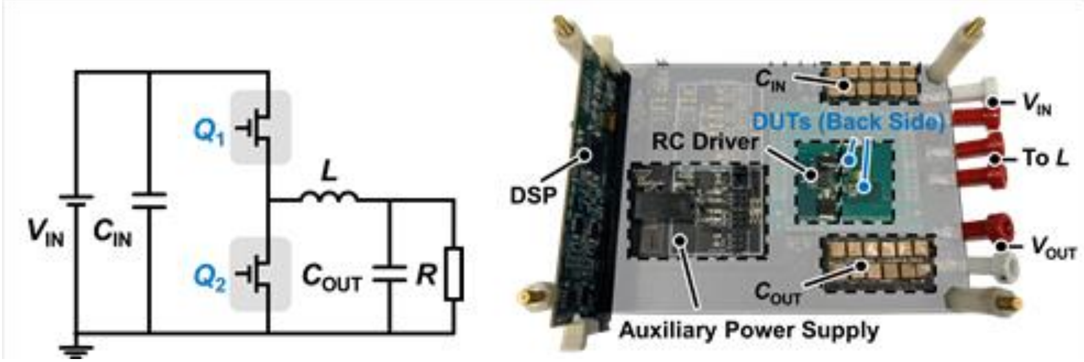




800V, 1MHz switching with wide *D* range



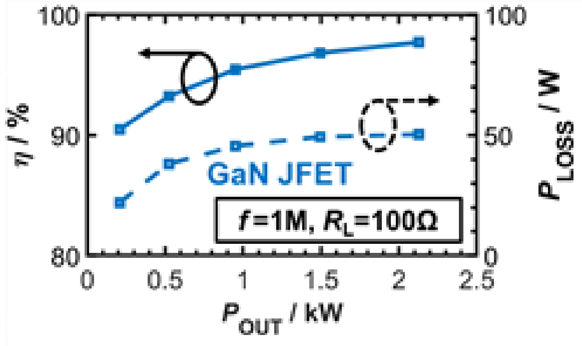
Zero-voltage-switching buck converter

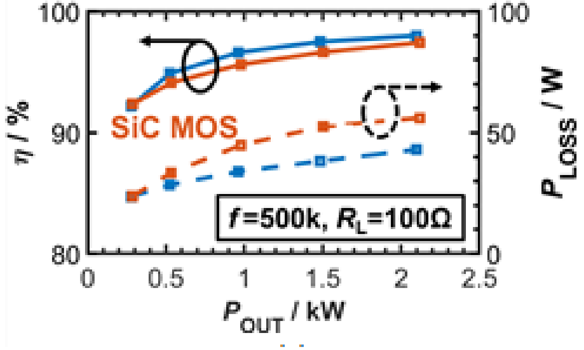


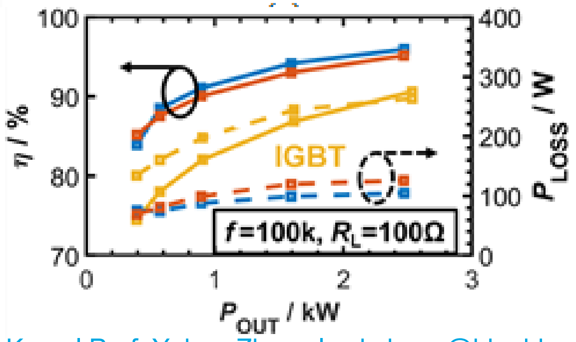
- turn-on loss >> turn-off loss
- zero dynamic R_{ON}

X. Yang *et al.*, “Evaluation and MHz Converter Application of 1.2-kV Vertical GaN JFET,” **T-PEL** 2024

Higher *f* and efficiency than SiC and Si FETs







50% smaller dead time

η=97.7% @1MHz

25% lower loss than SiC @500kHz

60% lower loss than Si @100kHz

NEXGEN POWER SYSTEMS

Summary

- **GaN reliability has to be evaluated in-situ under switching conditions**
- **Lateral GaN HEMT**
  - **Dynamic R_{ON} and C_{OSS} loss**
    - Different trapping origins (time constants); both can be suppressed by device engineering
  - **Overvoltage and surge-energy ruggedness**
    - *BV* is dynamic; dynamic R_{ON} could be the true limiter for overvoltage lifetime
  - **Gate reliability and switching lifetime**
    - New circuit method + switching lifetime model: arbitrary V_G waveform, T and f_{SW} dependence
- **GaN monolithic bidirectional switch:** new mission profiles and reliability issues
- **Vertical GaN JFET**
  - Dynamic R_{ON} free, better FOM than SiC MOS, robust avalanche and short-circuit